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HIGH-FILL-FACTOR 160 x 244-ELEMENT AND 320 X 244-ELEMENT PtSi SCHOTTKY-BARRIER IR-CCD IMAGE SENSORS

David Sarnoff Research Center

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Two high-fill-factor IR-CCD imagers, with PtSi Schottky-barrier detectors, were successfully demonstrated. The 160-element x 244-element imager has 80μm x 40μm pixels, with a fill factor of 60%, and a saturation signal of up to 2.5 x 10^5 electrons/pixel. For operation with a 300-K background, 30 frame/s, f/2.35 cold shield, and a 3.4μm long-pass filter, a noise equivalent temperature (NEΔT) of 0.04°C was measured for this imager.

The 320-element x 244-element imager has 40μm x 40μm pixels, a fill factor of 43%, and a saturation signal of up to 1.5 x 10^6 electrons/pixel. For operation with a 300K background, 30 frames/s, and f/2.0 cold shield, a shot-noise-limited NEΔT of 0.038°C was measured for this imager.

Both of the above imagers show no loss of horizontal and vertical resolution due to charge-transfer inefficiency for operation of the serial output register with a 2-phase CCD clock.

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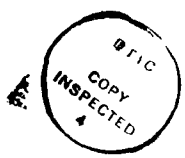
This report describes the design, processing, operation and performance of the new 160 x 244 and 320 x 244 IR-CCD imagers.



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PREFACE

This Final Report was prepared by the David Sarnoff Research Center, Princeton, NJ, under Contract No. F19628-85-C-0187. It describes work performed from 23 September 1985 to 30 September 1987, in the Optoelectronics Research Laboratory, M. Ettenberg, Director. The Project Supervisor was Dr. G. W. Hughes, Head of Optoelectronic Systems, and the Project Scientist was Dr. W. F. Kosonocky. Dr. F. V. Shallcross was responsible for processing of the focal plane arrays. The coding of the chip was done by G. M. Meray; the devices were processed by R. Miller and F. J. Tams; the electronics for operation of the arrays were developed by J. V. Groppe; and the array testing was done by T. S. Villani and J. J. O'Neill, III. The Air Force Technical Monitor was M. Weeks.

The manuscript of this report was submitted to Rome Air Development Center, Hanscom AFB, MA in February 1988.

Publication does not constitute Air Force approval of the findings or conclusions of this report. It is intended only for the exchange and stimulation of ideas.

1.0 INTRODUCTION

Metal-silicide photodiode-array technology was invented at Rome Air Development Center (RADC), Hanscom AFB, MA, and has been under development there since the early 1970s. In 1973, Shepherd and Yang proposed silicide Schottky-barrier detector (SBD) arrays for infrared thermal imaging [1, 2]. Since then, considerable progress has been made at the David Sarnoff Research Center, with the support of RADC, Hanscom AFB, on the development of Pd_2Si SBD image-sensor arrays for applications in the SWIR (1 to 3 μm) band and of PtSi SBD image-sensor arrays for thermal-imaging applications in the MWIR (3 to 5 μm) band [3-22]. Table 1 describes the Schottky-barrier IR-CCD focal plane arrays (FPAs) developed or under development at the David Sarnoff Research Center. Most of these FPAs were initially designed and fabricated with contract support from RADC, Hanscom AFB. Table 1 summarizes the chip sizes, the pixel sizes, the active detector areas, the fill factor (detector area efficiency), and the year of development for these arrays. With the exception of the 256 x 1, 512 x 2, and 512 x 22 line sensors, all of the area-sensing imagers have an interline-transfer-type organization.

The 25 x 50 and 256 x 1 IR-CCD FPAs were designed and initially fabricated at the David Sarnoff Research Center under contracts with RADC [3-6]. Initially, the FPAs were fabricated in 1978 with thick PtSi SBDs [2, 6]. The second area-sensing FPA developed at the David Sarnoff Research Center, with the support of RADC, Hanscom AFB, is the 32 x 63 IR-CCD FPA, TC1247 [7].

In 1979, the David Sarnoff Research Center, in a joint effort with RCA Automated Systems, Burlington, MA, achieved the initial breakthrough in the improvement of the sensitivity of the 25 x 50 IR-CCD FPAs by more than an order of magnitude. This improvement resulted from using a thin PtSi detector structure with an optical cavity. The first improved PtSi SBD structure evolved from our cooperative effort with Shepherd and Roosild from RADC, although the general concept of a thin SBD with an optical cavity was described in 1973 by Archer and Cohen for SBDs in the form of Au on p-type Si [24]. The development of this process for reproducible fabrication of high-performance PtSi SBDs, with further process optimization for improvements in sensitivity and responsivity/dark-current tradeoff, has been done as part of IR&D programs at

TABLE 1.
SCHOTTKY-BARRIER IR-CCD FOCAL PLANE ARRAYS DEVELOPED AT THE DAVID SARNOFF RESEARCH CENTER

Type of FPA	Chip Size	Pixel Size $(mil)^2$	Fill Factor μm^2 %	Type of SBD	Year of Development
25 x 50 TC1199	235 x 216	160 x 80	16	Pd_2Si PtSi	1975-1978
256 x 1 TC1256	438 x 71	40 x 200	50 to 83*	PtSi	1975-1979
32 x 63 TC1247	265 x 265	160 x 80	25	PtSi Pd_2Si	1980/1981 1981-1982
64 x 128 TC1266	364 x 364	120 x 60	20 (33)	PtSi	1981/1982
64 x 128 TA11367 and TA11940	268 x 272	80 x 40	29 to 44* 39	PtSi	1983/1984 1984/1985
160 x 244 TA11524	584 x 464	80 x 40	39	PtSi	1983/1984
512 x 2 TA11567 2-side buttable	607 x 146	30 x 30	70 to 87*	Pd_2Si PtSi	1983-1985 1986
100 x 100 FT-CCD DSI TC1253	324 x 326	50 x 50	100	PtSi	1984/1985
128 x 128 IT-CCD DSI TA13014	350 x 350	50 x 50	100	PtSi	1985/1986
512 x 22 TA13314A	694 x 656	36 x 30	120	PtSi	1985/1986
512 x 2 TA13346A	694 x 157	36 x 30	120	PtSi	1985/1987
512 x 16 TA13373A CSD TDI 2-side buttable	605 x 415	30 x 30	50 (Horz.) 25 (Effective)	PtSi	1986-1987
160 x 244 TA13401A	584 x 464	80 x 40	60	PtSi	1986/1987
320 x 244 TA13401B	584 x 464	40 x 40	43	PtSi	1986/1987

*Fill factor depends on design option.

the David Sarnoff Research Center from 1980 through 1986 [8-19]. The 32 x 63 IR-CCD FPA, the two 64 x 128 IR-CCD FPAs (TC1266 and TA11367), and the 160 x 244 IR-CCD FPA (TA11524) were used in the above effort.

The 64 x 128 (TA11367) and 160 x 244 (TA11524) IR-CCD FPAs were designed and developed at the David Sarnoff Research Center under a contract from RADC, Hanscom AFB, MA, from July 1981 to September 1984 [14-19]. Both of these IR-CCD FPAs have the same basic design in the form of an interline-transfer IR-CCD imager with 2:1 vertical interlacing. The 64 x 128 IR-CCD FPA (TA11940) is a version of the TA11367 device, with a 39% fill factor representing process improvement introduced in 1984.

The 512 x 2 Pd_2Si IR-CCD dual-line sensor (TA11567) has been developed as part of a joint effort of RCA Advanced Technology Laboratories, Moorestown, NJ, and the David Sarnoff Research Center, under a contract with NASA Goddard Space Center, Greenbelt, MD [20, 21]. The development of Pd_2Si SBDs, for operation at 1.24- to 2.22-μm wavelengths and passive cooling at 120 K, was done at the David Sarnoff Research Center as part of 1983 to 1986 IR&D programs.

In 1983, the David Sarnoff Research Center initiated a research effort on the development of Direct Schottky Injection (DSI) FPAs that have 100% fill factors. The DSI FPAs are constructed with a continuous PtSi Schottky-barrier surface on one side of a thinned silicon substrate, with the CCD readout register formed on the other side. In 1984, we demonstrated the DSI concept with the 100-x 100-element frame-transfer CCD DSI imager (TC1253), and we also initiated the development of a 128 x 128 interline-transfer CCD DSI imager with 50-μm x 50-μm pixels. Excellent quality of thermal imaging, with NEΔT of 0.04 K, was demonstrated in 1986 with the 128 x 128 IT-CCD DSI imager [22].

As part of the 1985 and 1986 IR&D efforts, the David Sarnoff Research Center designed and fabricated a 512 x 22 multi-line sensor (TA13314A) with 36-μm (H) x 30-μm (V) staggered pixels. This FPA was made for a space-surveillance demonstration camera in the RCA Astro-Electronics Division. The TA13314A wafers also included, as knockout, the following arrays:

(1) A 512 x 2 line sensor with 30-μm x 30-μm pixels having 120% fill factor in the form of staggered detectors (TA13346A)

(2) A high-speed version of the TA11567 512 x 2 line sensor with 30-μm x 30-μm pixels and 70% fill factor

(3) A 512 x 16 TDI two-side buttable TDI array (TA13373A) with a charge-sweep-device (CSD) readout [23]

The 160 x 244 IR-CCD FPA (TA13401A) with 80-μm x 40-μm pixels and 60% fill factor, and the 320 x 244 IR-CCD image sensor (TA13401B) with 40-μm x 40-μm pixels and 43% fill factor were developed under this program at the David Sarnoff Research Center, Princeton, NJ, with the support of the Rome Air Development Center, Solid State Science Division, Hanscom AFB. These results are described in this Final Report. These FPAs were designed to have the same chip size and to be essentially pin-for-pin compatible with the previously developed 160 x 244 IR-CCD FPA (TA11524) [15, 19]. The only difference in terms of the pin-out is that, while the 160 x 244 TA11524 FPA has a serial input register, the high-fill-factor 160 x 244 and the 320 x 244 FPAs were designed without the serial input register. Therefore, the high-fill-factor FPAs do not have the bonding pads corresponding to the input register of the TA11524 FPA.

2.0 DESIGN AND CONSTRUCTION OF THE HIGH-FILL-FACTOR IR-CCD FPAS

2.1 CHIP DESCRIPTION

The 160 x 244 FPA (TA13401A) with 80-μm (H) x 40-μm (V) pixels and 60% fill factor and the 320 x 244 FPA (TA13401B) with 40-μm x 40-μm pixels and 43% fill factor both developed under the program, were designed to be pin-for-pin compatible and package-compatible with the original 160 x 244 FPA (TA11524) with 80-μm (V) x 40-μm (V) pixels and 39% fill factor [15, 19]. All three of the above FPAs have the same chip size of 584-mil x 464-mil, and the photosensitive area of these imagers has a standard TV aspect ratio of 4(H):3(V). Similar to the original 160 x 244 FPA (TA11524), the high-fill-factor 160 x 244 FPA and the 320 x 244 FPA are interline-transfer IR-CCD imagers designed for operation with a readout of two vertically interlaced fields/frame. This design allows a rather area-efficient pixel construction, with two-level polysilicon gates, by using 4-phase (double-clocked) operation of the IR-CCD area sensor.* The new high-fill-factor FPAs, however, were designed with smaller design rules (corresponding to 2.5-μm minimum feature sizes and ±1.0-μm alignments) and have no input register. The CCD input register, used mainly for electrical testing of the TA11524 FPAs, was removed to allow introduction of vertical aluminum busses (one for each column register) for reduction of the RC time constant of the parallel B clock and to provide redundant connections for the vertical column gates.

A schematic layout, with 4 x 4 pixels, of the high-fill-factor 160-element x 244-element FPA and the 320 x 244 FPA, is shown in Fig. 1. The construction of these FPAs is further illustrated by the checkplots in Figs. 2 and 3 and the photographs of the output sections in Figs. 4(a) and (b). The construction of the pixels of these two FPAs is also illustrated by the SEM photographs in Figs. 5(a) and (b), showing a half-stage of the CCD register and the corresponding Schottky-barrier detector after definition of the SBD contacts. The SEM photographs of these pixels, after the completion of the processing after the aluminum definition, are shown in Figs. 6(a) and (b).

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* In 4-phase, double-clocked operation, the CCD well always extends under at least two adjacent transfer gates.

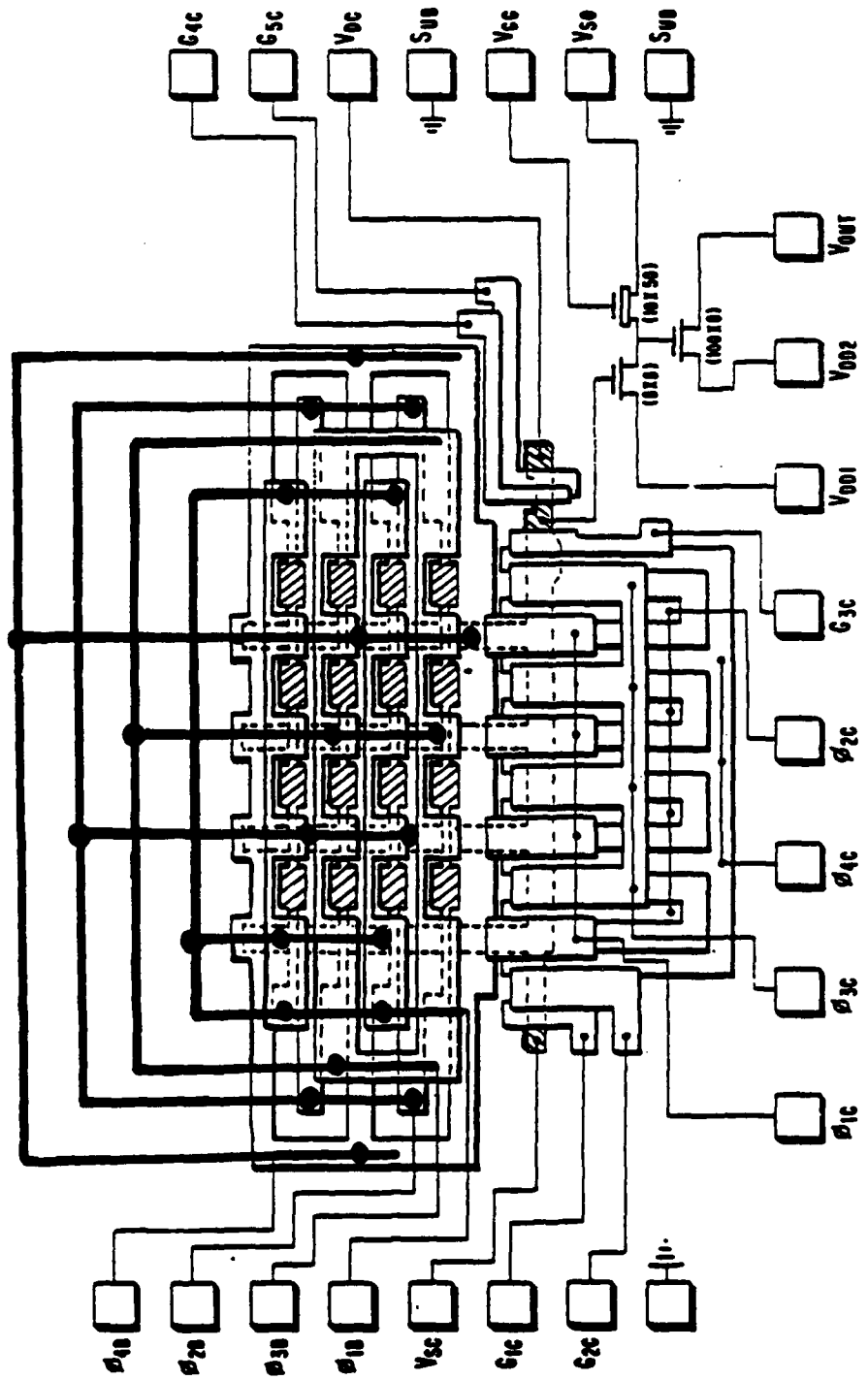


Figure 1. Schematic layout of 160 x 244 IR-CCD FPA (TA13401A) and 320 x 244 IR-CCD FPA (TA13401B).

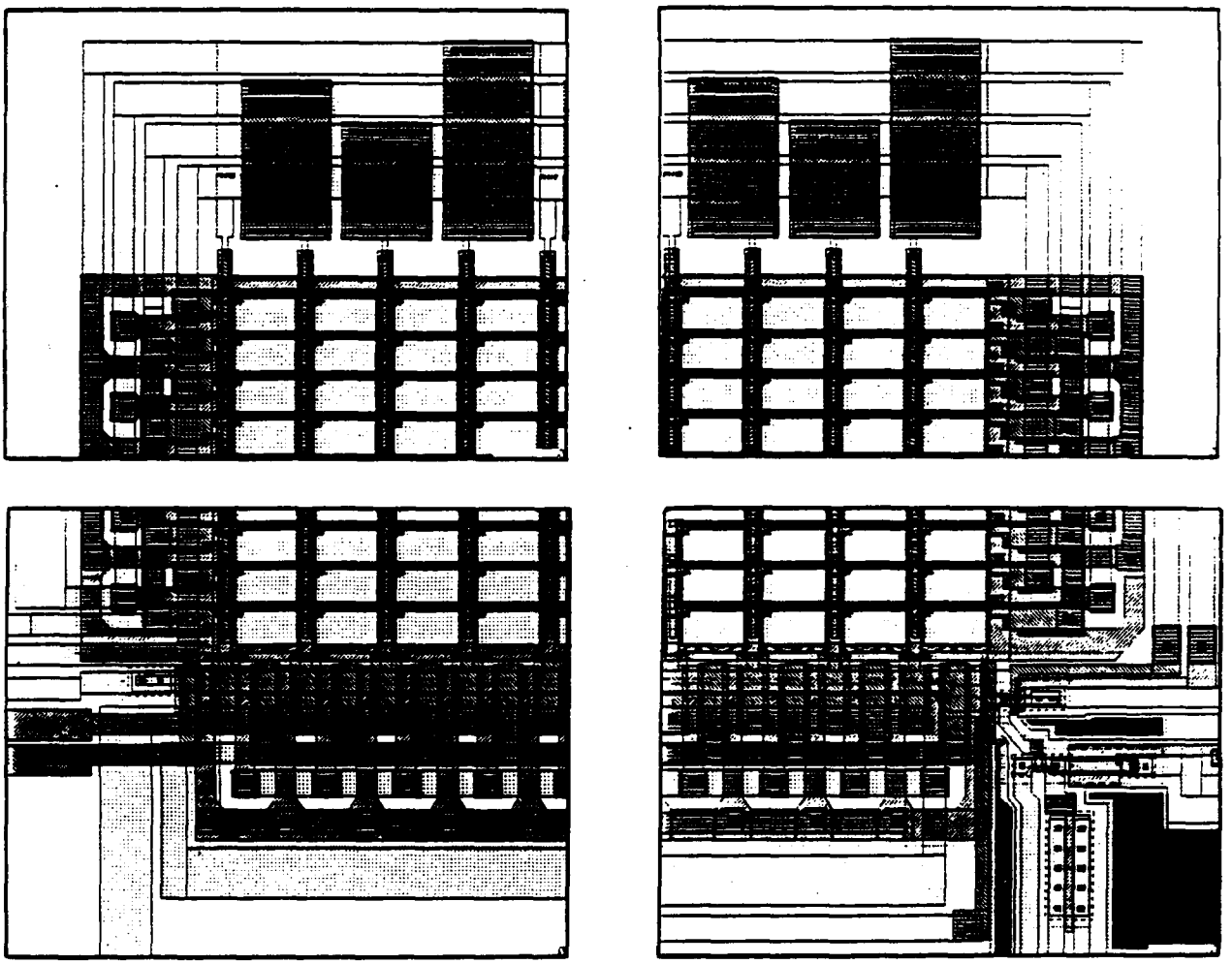


Figure 2. **Checkplot of the 160 x 244 IR-CCD imager with 80-μm x 40-μm pixels and 60% fill factor.**

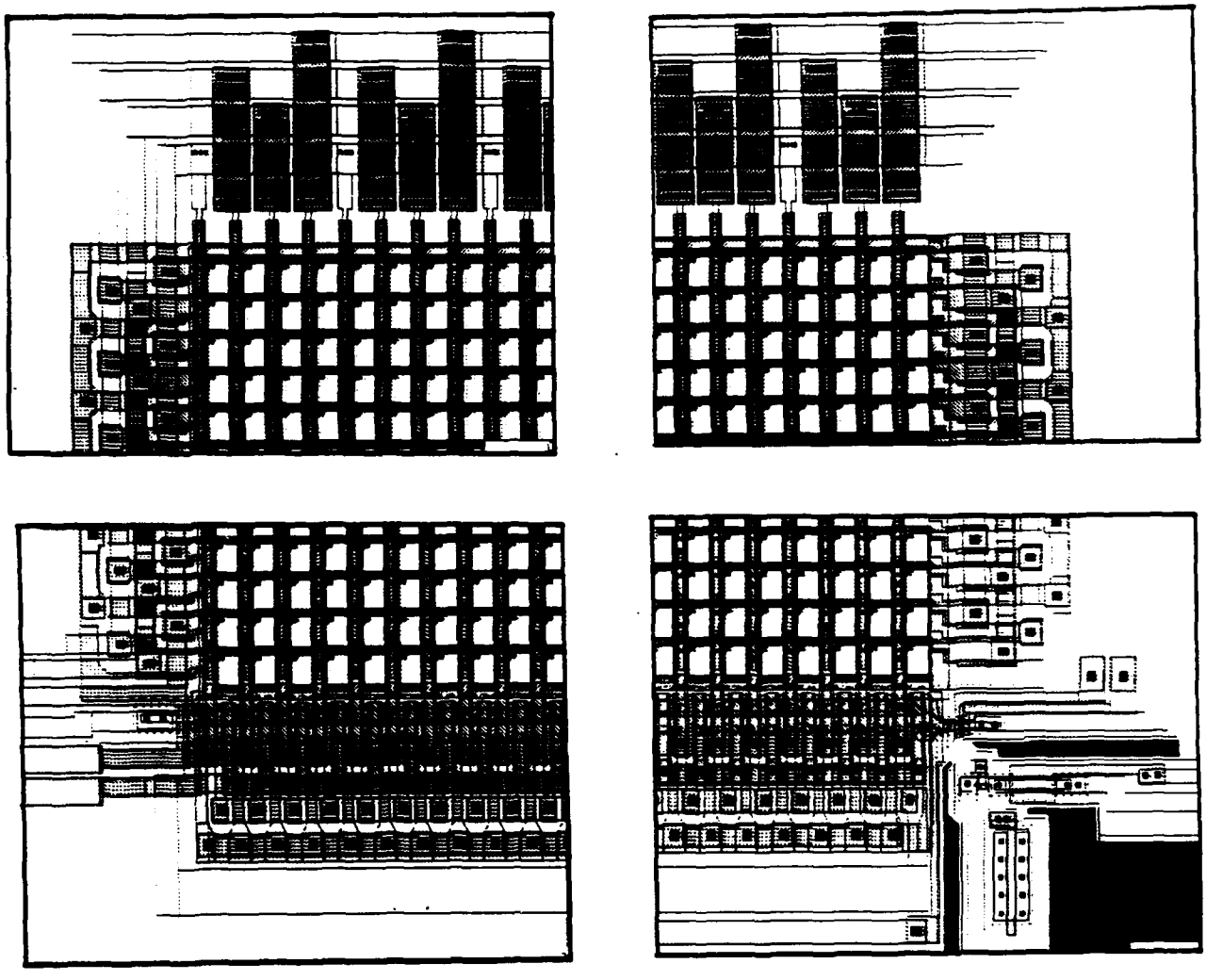


Figure 3. Checkplot of the 320 x 244 IR-CCD imager with 40-μm x 40-μm pixels and 43% fill factor.

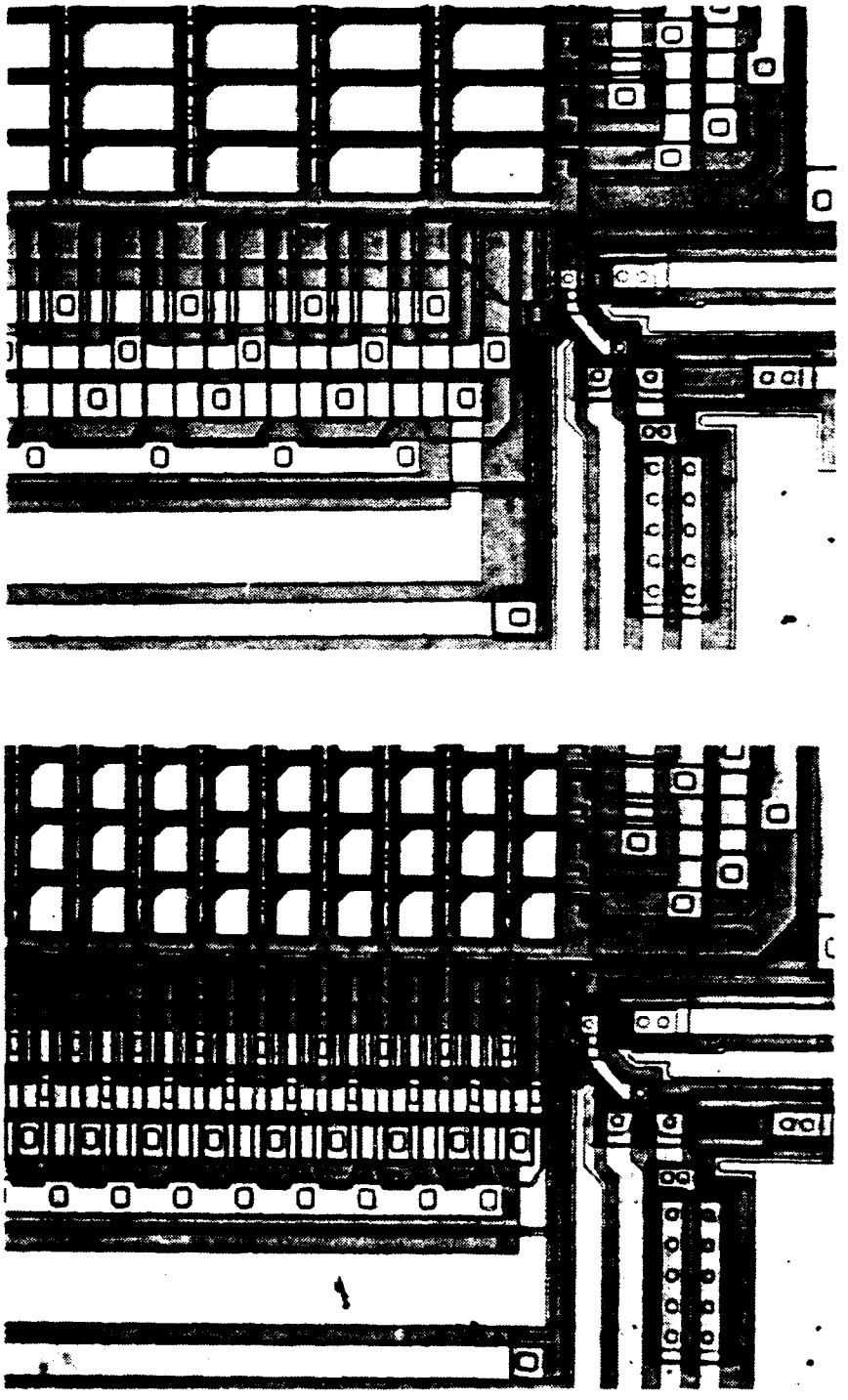
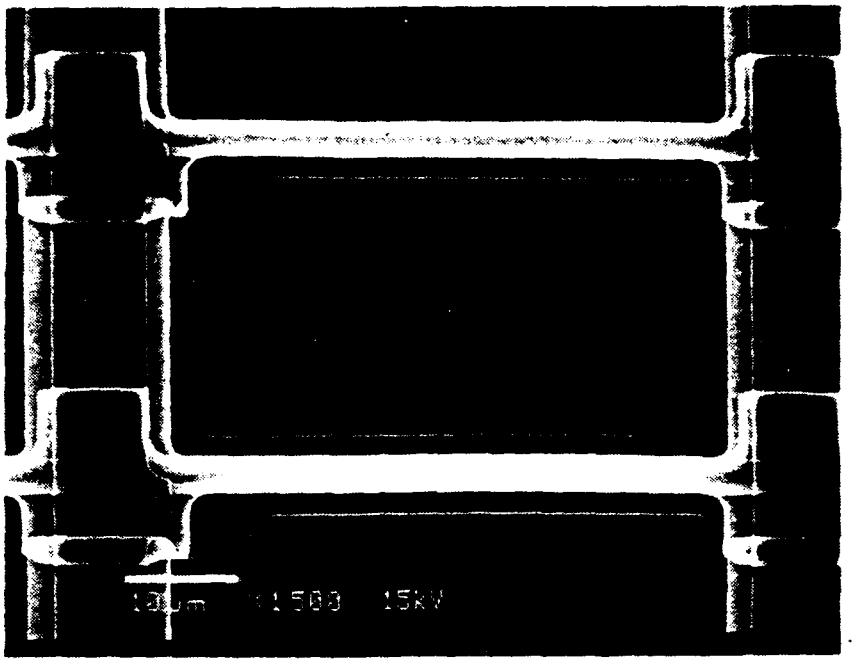
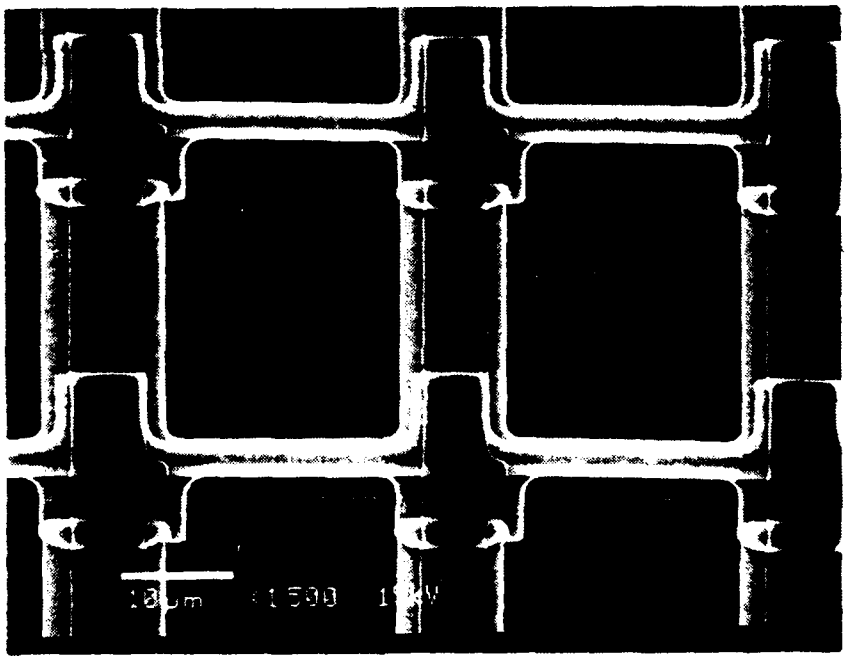


Figure 4. Photomicrographs of the output section of the 160 x 244 IR-CCD FPA (TA13401A) in (a) and of the 320 x 244 IR-CCD FPA (TA13401B) in (b).

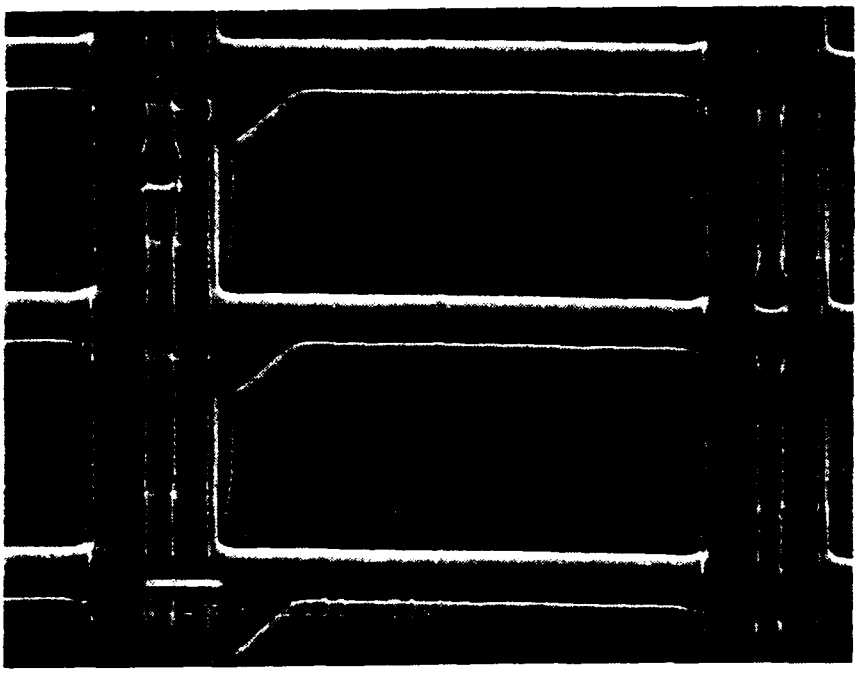


(a)

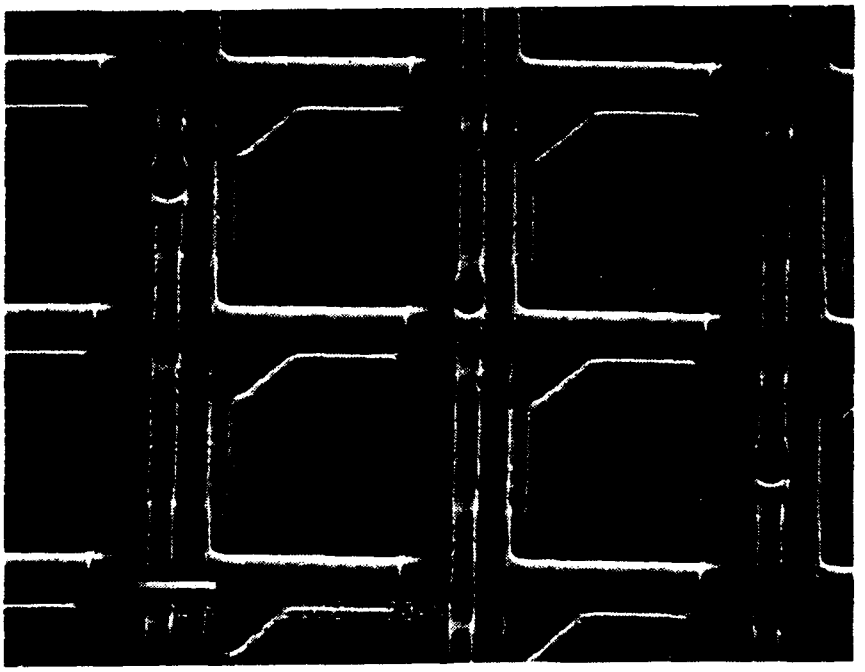


(b)

Figure 5. SEM photographs, at 30° illustrating the construction of the pixels after the definition of the SBD contacts for the 80-μm x 40-μm pixels in (a) and the 40-μm x 40-μm pixels in (b).



(a)



(b)

Figure 6. SEM photographs, at 30°, of a pixel after definition of aluminum for the 80-μm x 40-μm pixel in (a) and the 40-μm x 40-μm pixel in (b).

Returning to the checkplots in Figs. 2 and 3, the connections to the vertical aluminum busses that strap CCD gates of the 4-phase parallel B register are facilitated by tunnels in the form of the two-layer polysilicon connections shown on the top of these figures.

The serial output C register for these FPAs, shown in Figs. 1 through 3, was designed for a 4-phase operation with 20-μm-long gates in the case of the 160 x 244 FPA, and 10-μm-long gates in the case of the 320 x 244 FPA.* The serial output registers of both FPAs have a BCCD-1 channel with a width of 12 μm, which also includes a deeper BCCD-2 channel (trench) of 3 μm, as shown in Fig. 7. The deeper CCD-channel BCCD-2 implant was introduced for these FPAs to decrease the charge-transfer losses at low signal levels that can be contained by the 3-μm channel [26]. Also, both FPAs were designed, with the C-register readout by the same type of on-chip, two-stage source-follower amplifier with a floating-diffusion sensing-node capacitance of 0.04 pF and a measured charge-to-voltage transfer gain of 350 electrons/mV or 2.8 μV/electron. The two-stage, source-follower, on-chip amplifier (see Fig. 1) has a surface-channel input MOSFET with an 8-μm x 8-μm channel, a 50-μm-long and 10-μm-wide buried-channel load device; and a 8-μm-long and 100-μm-wide surface-channel output MOSFET. The photomicrographs of the chips of the new 160 x 244 FPA and the 320 x 244 FPA are shown in Figs. 8 and 9. Inspection of Fig. 8 shows that the 160 x 244 IR-CCD FPA (TA13401A) contains no test devices (as specified by RADC). The pattern included on the top edge of this chip is for alignment marks. All of the test devices for process control and device characterization were included at the perimeter of the 320 x 244 FPA (see Fig. 9). The layout of seventeen 160 x 244 FPAs and fourteen 320 x 244 FPAs on a 4-in. silicon wafer is shown in Fig. 10. The 160 x 244 and 320 x 244 FPAs were bonded in specially designed 32-pin ceramic packages shown in Fig. 11. This package is designed for introduction of the optical signal through a 544-mil x 424-mil window.

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* As described in Sections 3.1 and 3.2.3, the C registers of these FPAs were operated with a 2-phase clock since this form of operation results in considerably lower charge-transfer inefficiency.

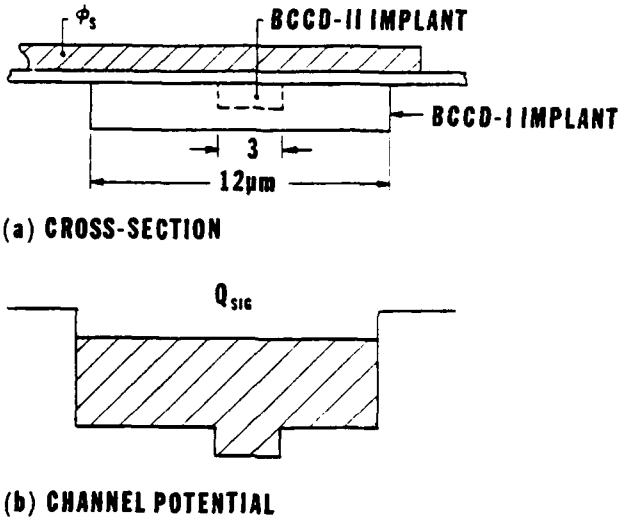

Figure 7. Cross-section of the serial output register.

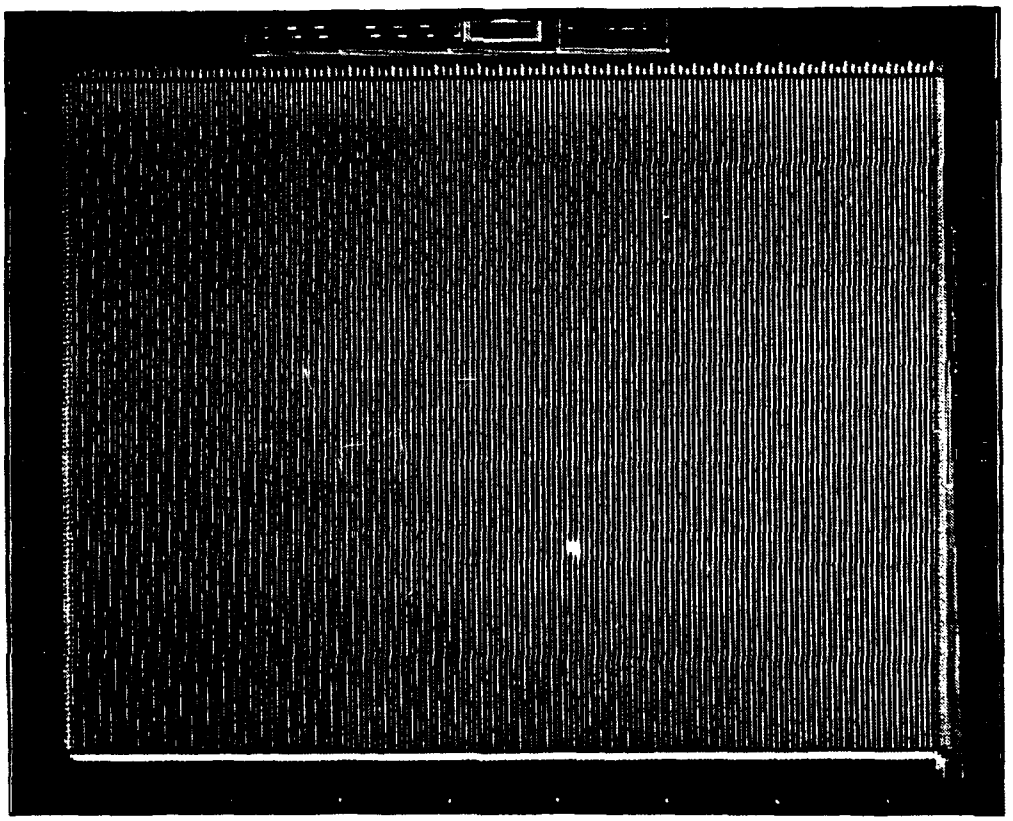

Figure 8. Photomicrographs of the 160 x 244 FPA chip.

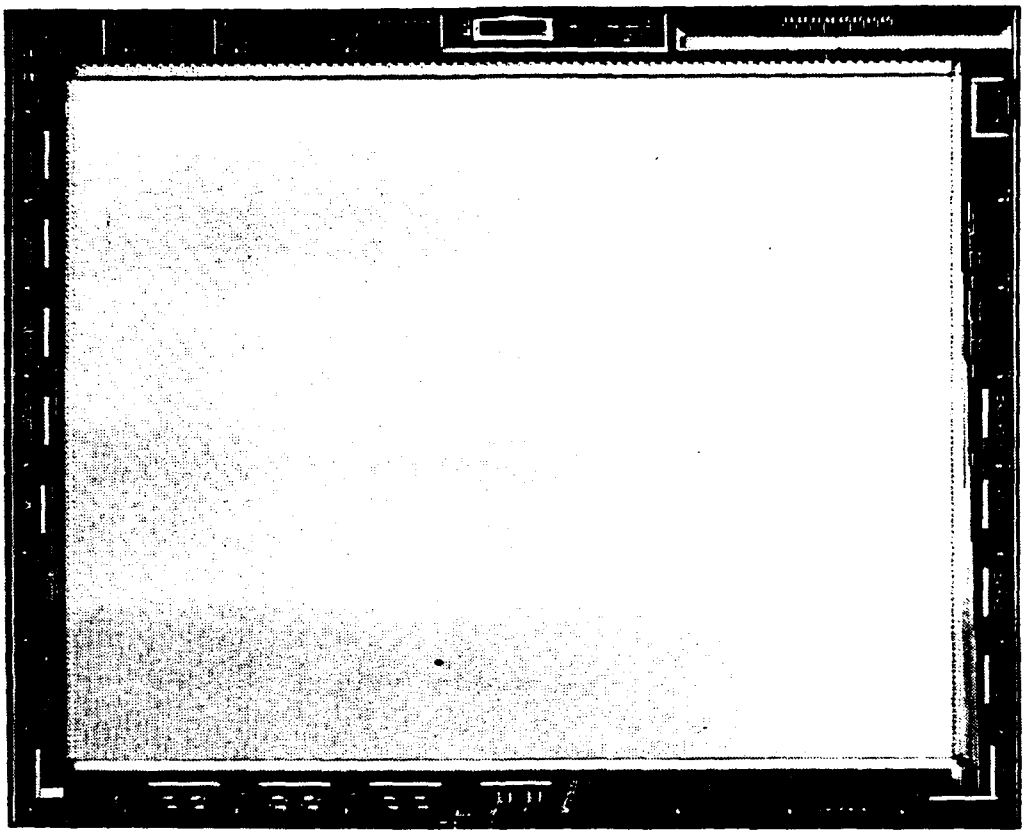

Figure 9. Photomicrograph of the 320 x 244 FPA chip.

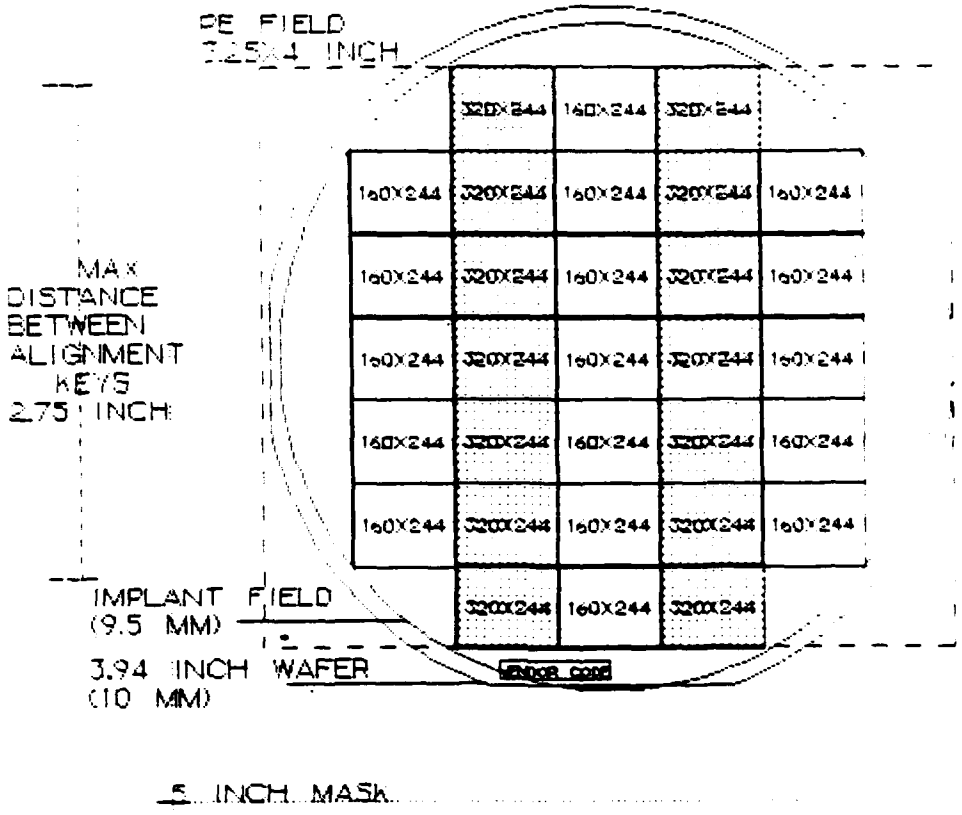

Figure 10. Layout of 160 x 244 and 320 x 244 IR-CCD imagers on a 4-in. silicon wafer.

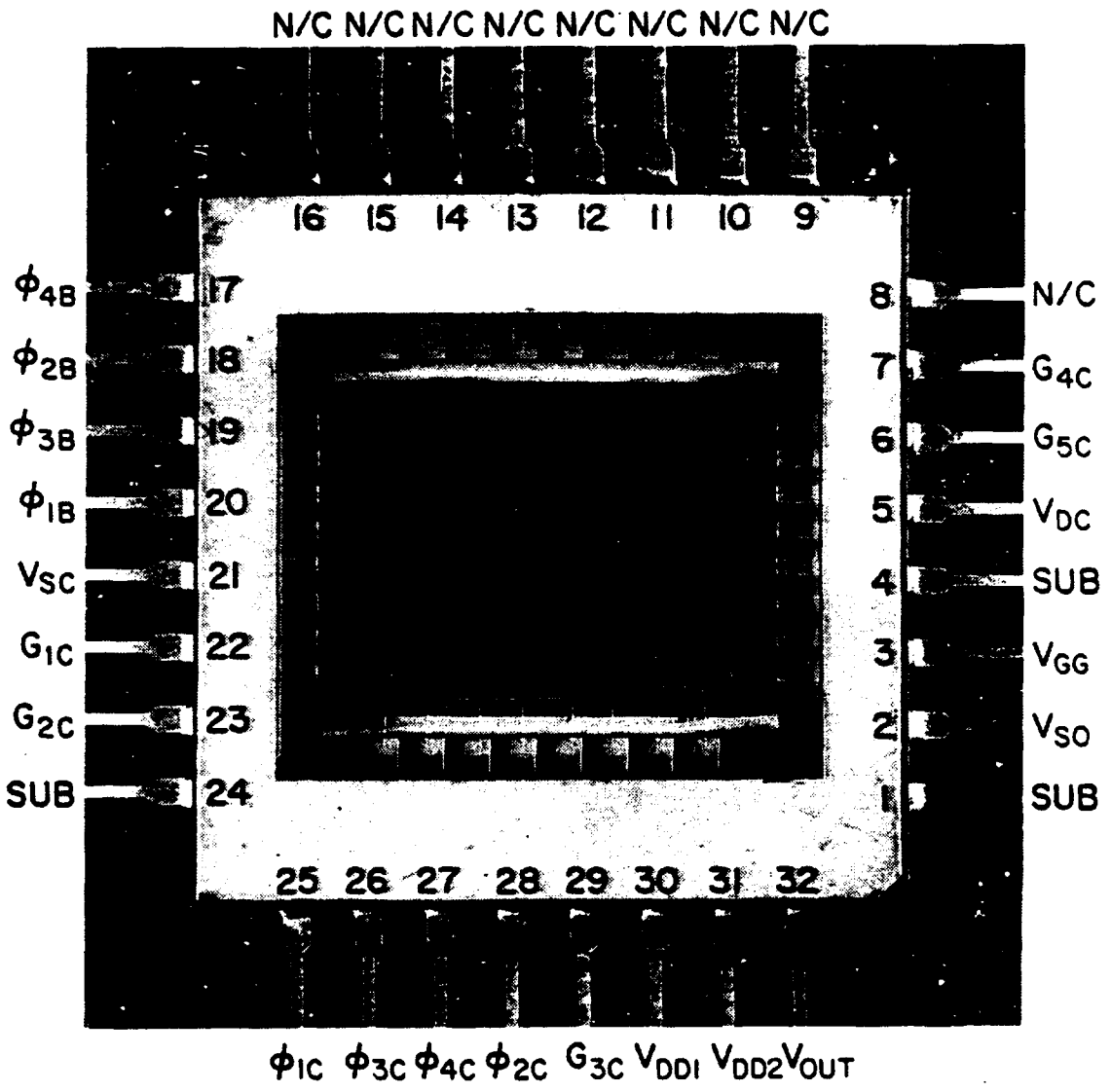

Figure 11. A 320 x 244 IR-CCD imager bonded in a 32-pin ceramic package.

2.2 PIXEL DESIGN

The main objective of this program was to increase the fill factor of the 160 x 244 FPA, with 80-μm x 40-μm pixels, from 39% to 60% while maintaining the charge-handling capacity of the CCD readout multiplexer, which it was at least 2 x 10^6 electrons/pixel. This was achieved for fabrication of the arrays by the Perkin-Elmer 1:1 projection microaligner, with minimum design rules of 2.5 μm and ±1.0-μm alignment tolerances, by using the self-aligned IR-CCD process described in Section 3.2.1 [27]. The layout of the 80-μm (H) x 40-μm (V) pixels for the 160 x 244 FPA with a 60% fill factor is shown in Fig. 12. The required increase

of the fill factor from 39% to 60% was achieved by reducing the n^+ guard rings from 4.0 to 2.0 μm, the width of the p-type channel stops between buried-channel CCD (BCCD) register and the Schottky-barrier-detector (SBD) guard ring from 6 to 2.5 μm, and the width of the polysilicon-gate connections between the SBDs from 7 to 4 μm. By maintaining the width of the BCCD-readout register at 10 μm, we have satisfied the charge-handling capacity requirement. The active area of the pixel, corresponding to the inside dimensions for the n^+ SBD guard rings, is (61-32) μm^2 - 40 μm^2, resulting in a nominal fill factor of 60%.* (The area of 40 μm^2 corresponds to the region associated with the SBD readout.)

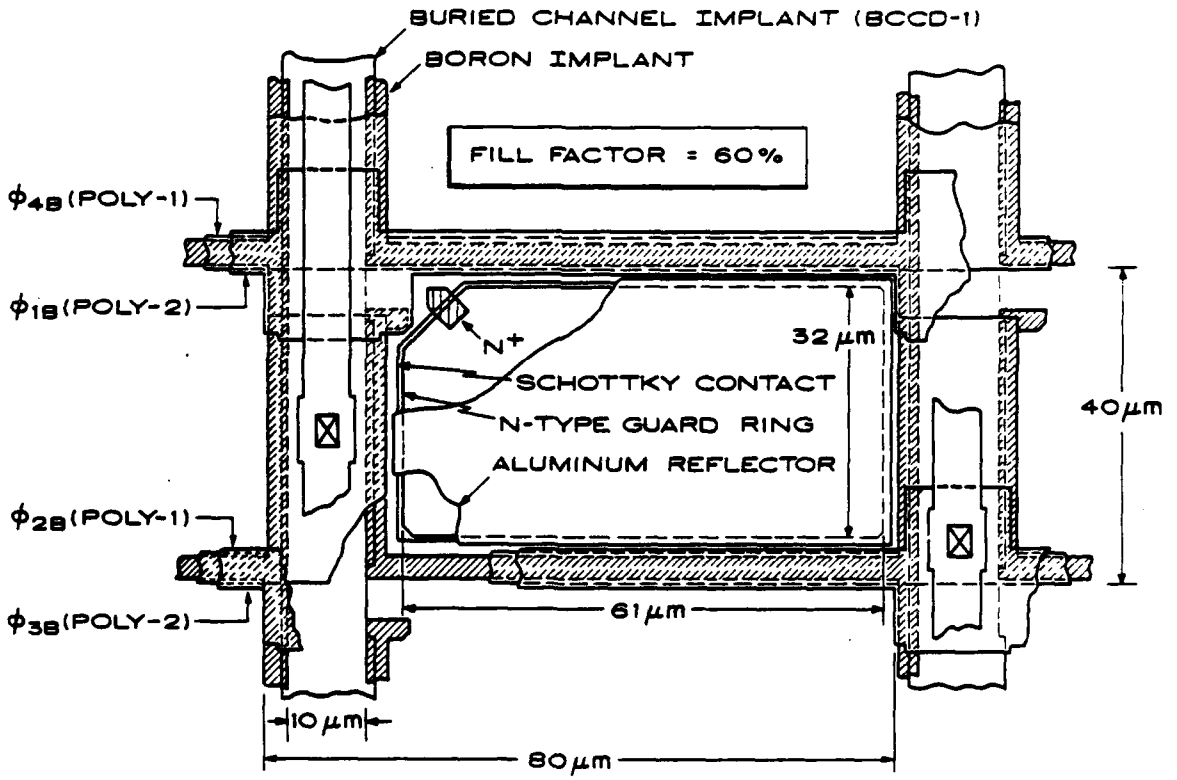

Figure 12. Layout of the 160 x 244 FPAs 80-μm x 40-μm pixel with a 60% fill factor.

The pixel layout in Fig. 12 shows one half-stage of the BCCD readout register with a 34-μm-long poly-1 gate corresponding to either $Ø_{2B}$ or $Ø_{4B}$, a 6-μm-long poly-2 gate corresponding to either $Ø_{1B}$ or $Ø_{3B}$, and a 5-μm-long and 6-μm-wide surface-channel (SCCD) transfer region between the N^+ SBD guard ring and

* The actual fill factor may be reduced by the diffusion of the N^+ guard ring and its definition.

the BCCD channel. The n^+ diffusion shown in Fig. 12 has been introduced to ensure a good ohmic contact between the n^+ guard ring, self-aligned to the polysilicon gates, and PtSi electrode of the SBD.

The pixel design of the 320 x 244 FPA with 40-μm x 40-μm pixels and a fill factor of 43% is shown in Fig. 13. This pixel layout uses the same basic design as the 80-μm x 40-μm pixels with a 60% fill factor shown in Fig. 12, except that the width of the BCCD readout register was reduced from 10 to 7 μm, and the p-type channel stops between the SBD guard rings were increased from 2.5 to 3.0 μm. Thus, the resulting horizontal dimension of the active SBD area was reduced from 61 to 23 μm.

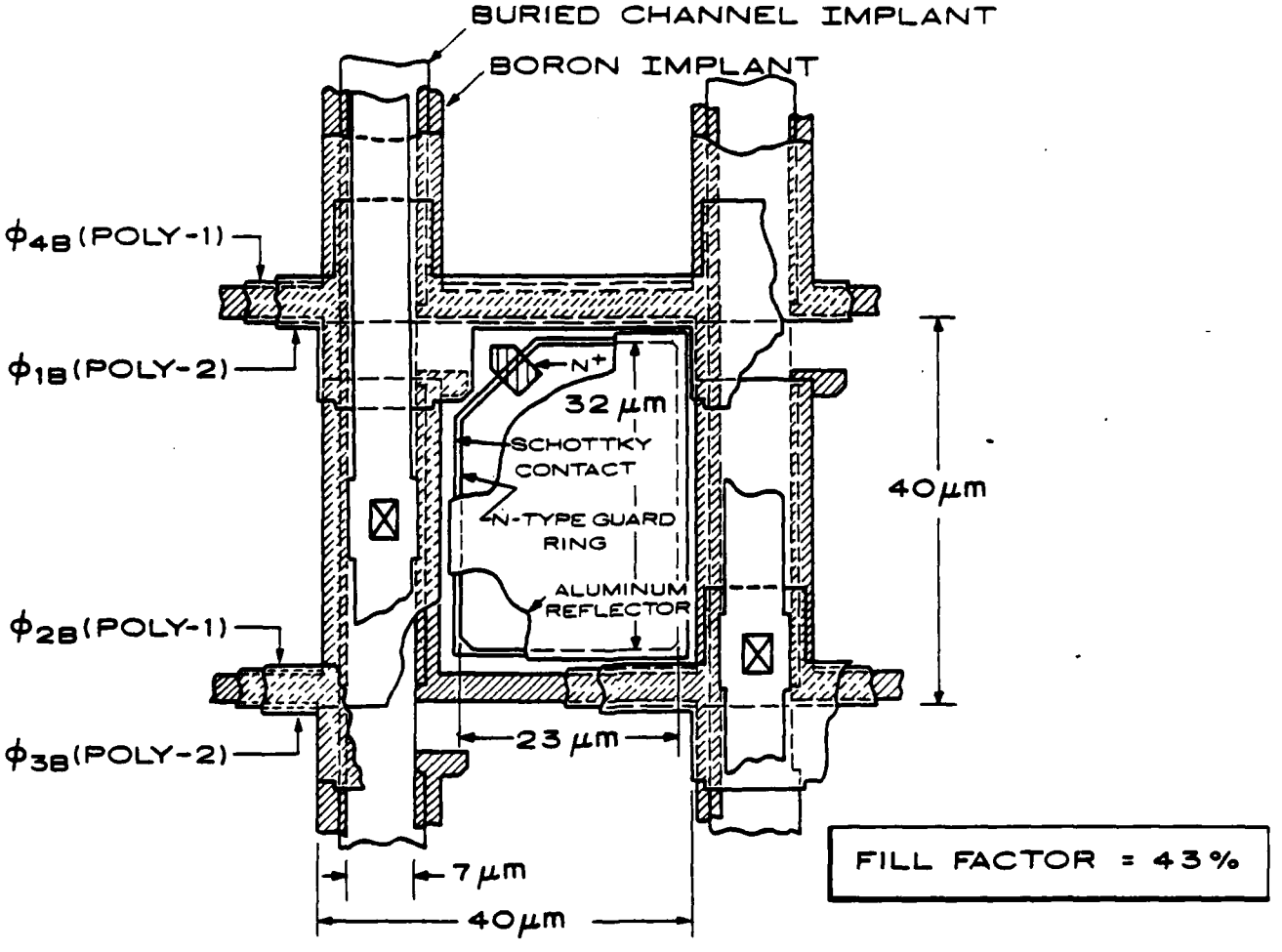

Figure 13. Layout of the 320 x 244 FPAs 40-μm x 40-μm pixel with a 43% fill factor.

2.3 PIXEL CONSTRUCTION AND SBD READOUT

The construction and operation of the SBD with a CCD readout is illustrated in Fig. 14. The construction of these pixels is further illustrated by the cross-section view (shown not to scale) in Fig. 14 (a). In this construction, the SBDs are contained on all four sides by one or two levels of polysilicon gates. To minimize dark-current spikes, the PtSi SBDs are surrounded by n^+ guard rings self-aligned to the polysilicon gates. The channel stops, between two adjacent SBDs in the vertical direction and the SBDs and buried-channel CCD (BCCD) readout registers, are in the form of 2.5-μm-wide, p-type implanted regions and a 5-μm-long and 6-μm-wide surface-channel CCD (SCCD) transfer region between the SBD and the BCCD readout register.

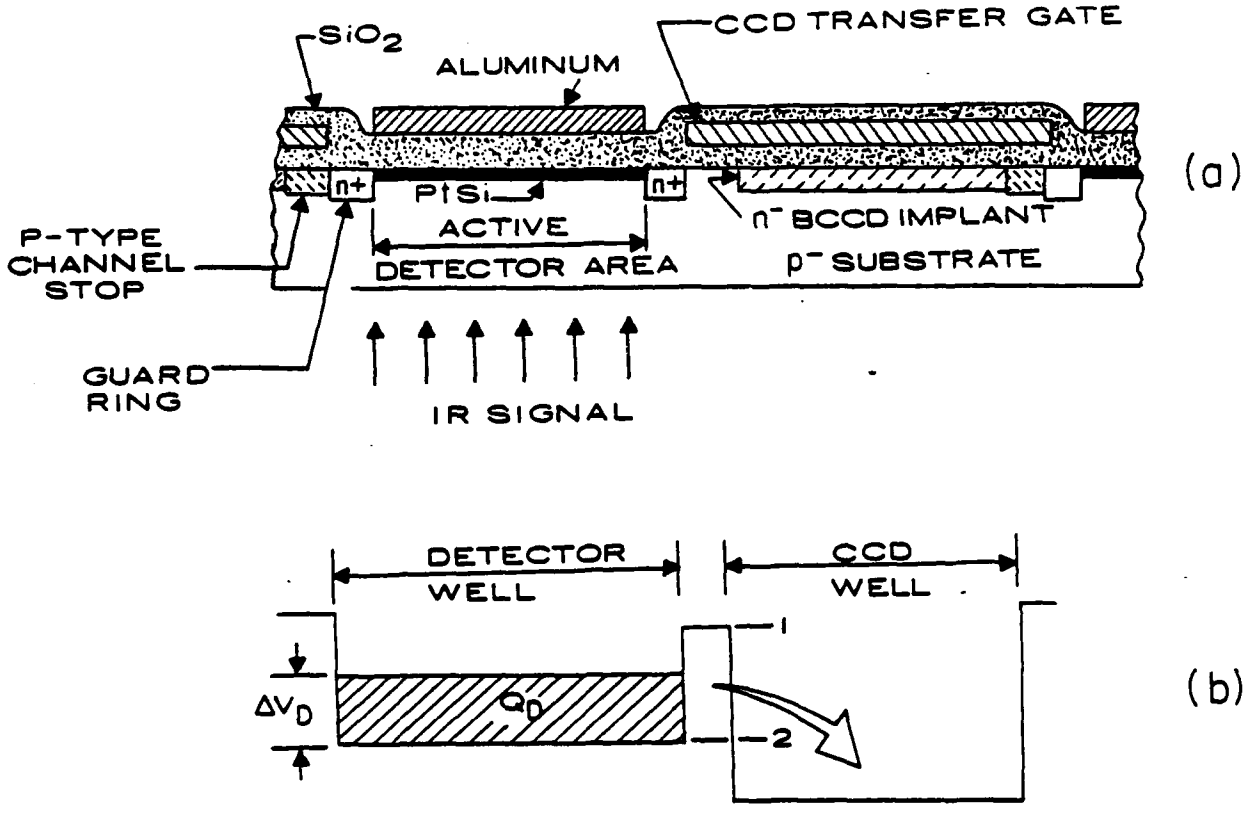

Figure 14. Construction and operation of the SBD with CCD readout.

As illustrated by the channel potentials in Fig. 15, the SCCD channel stops are driven into accumulation by the B clock ($\Delta\emptyset_B$) during the CCD-charge-transfer operation of the B register. At the end of the optical integration time (T_i),

the CCD-transfer gate $\emptyset_{1B}$ (or $\emptyset_{3B}$) is driven to a positive potential V_{BT}, as illustrated in Figs. 14 (b) and 15. This operation resets the SBD electrode to reference potential-2, as shown in Fig. 14 (b), corresponding to $\Psi_{T\text{-}SCCD}$ (Fig. 15), and transfers the detected charge signal (Q_D) into the CCD well. During this charge transfer, a higher barrier potential is formed under the p-type channel stops shown in Figs. 12, 13, and 14 (a). This barrier provides the directionality of the signal-charge flow during the SBD charge readout.

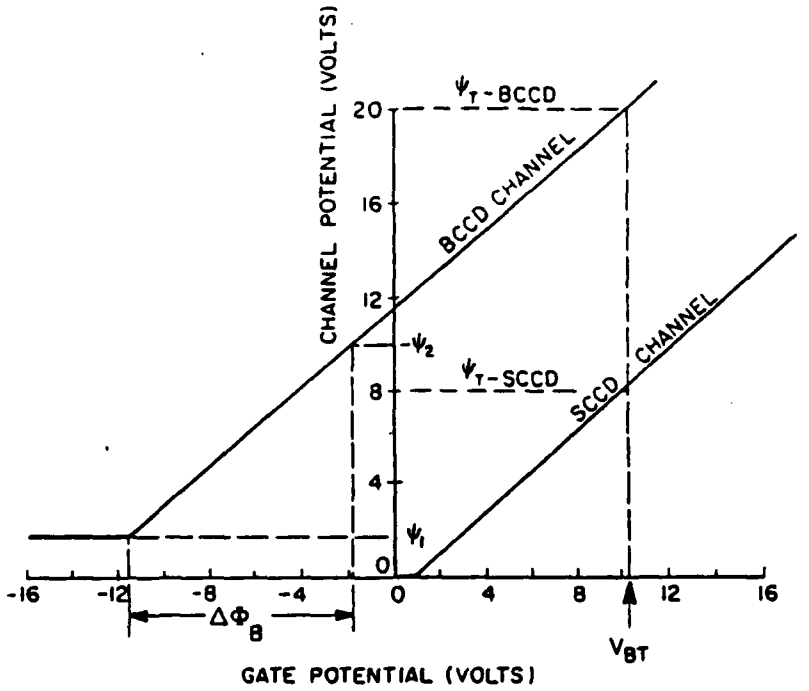

Figure 15. Curves of the channel potential vs gate voltage for a buried-channel CCD, and a surface-channel CCD illustrating the operation of the SBD readout in Fig. 14.

The operation of the SCCD channel-stop regions into accumulation ensures an operational blooming control mode of the SBDs, provided the BCCD readout register has a sufficient charge-handling capacity [6, 9, 15, 19]. The built-in blooming control of the Schottky-barrier detector functions as follows: A strong optical signal forward-biases the SBD, and no further negative charge is accumulated at the PtSi electrode. The small negative voltage developed at the PtSi electrode is not sufficient to forward-bias the n^+ diffusion of the detector. Therefore, no negative charge can pass under the surface channel portion of the transfer gate and be injected into the CCD register.

2.4 DEVICE FABRICATION

2.4.1 Self-Aligned IR-CCD Process

The high-fill-factor 160 x 244 and 320 x 244 FPAs were fabricated with the 13-mask self-aligned IR-CCD process [27] shown in Table 2. The self-aligned features of this process allowed us to achieve the required 60% fill factor for the 160 x 244 FPAs, using 2.5-μm minimum features and ±1.0-μm alignment tolerances available with the Perkin-Elmer 1:1 projection aligner. This process consists of the following major steps:

(1) The process is started with a 7000-Å-thick, thermally grown SiO_2 field oxide. This field oxide is progressively removed by the first four mask steps (M1 to M2).

(2) The boron implant mask (M1) is used as the reference for masks M2 to M6. As shown in Fig. 16 (a), this masking step defines the boron implant for the 2.5-μm p-type channel stops between the buried-channel (BCCD) column register and the SBDs, and the 3-μm channel stops between two adjacent SBDs.

(3) As shown in Fig. 16 (b), the buried-channel implant-1 (M2) is self-aligned with the M1 pattern having a net p-type doping at the p-barriers.

(4) The p^+ diffusion channel stops and the substrate are defined by the M3 mask, while the SBD detector regions are still covered by the 7000-Å-thick field oxide.

(5) The channel oxide regions are defined by the field oxide mask M4, which also removes the field oxide from the SBD regions.

(6) The buried-channel-2 implant is defined by a photoresist placed over a thin, thermally grown SiO_2 in the CCD channel regions.

(7) After definition of the first-level-polysilicon gates (M6) and the second-level polysilicon gates (M7), a nitride (Si_3N_4) masking level is used to define 2-μm-wide n^+ guard rings and to grow about 5000-Å-thick SiO_2 over the n^+ guard rings and 2-μm-wide edges of the polysilicon gates, as shown in Figs. 17 (a) and (b). In this process, the n^+ guard rings are self-aligned to the polysilicon gates.

(8) The n^+ diffusion mask (M9), as shown in Figs. 12 and 13, is used to make an ohmic contact to the SBD silicide and to provide an electrical continuity from the SBD to the n^+ guard ring which is also self-aligned to the polysilicon gates.

(9) After deposition of the BPSG reflow glass, definition of the contacts to the diffusion, polysilicon gates, and p^+ substrate regions, the BPSG in the contact regions is reflown.

(10) During the opening of the SBD contacts, illustrated in Fig. 18, the 5000-Å SiO_2 oxide, originally self-aligned with the nitride mask, protects the polysilicon insulation during the SBD contact step and also provides a self-alignment of the SBD contacts to the n^+ guard rings.

(11) The formation of the Schottky-barrier detectors is accomplished by deposition of Pt, formation of PtSi, deposition of the SiO_2 SBD dielectric, definition of the SBD dielectric by the M12 mask, deposition of aluminum, and definition of the aluminum SBD reflectors by the metallization mask M13. The mask M13, which completes the processing sequence, also defines all of the aluminum interconnects for the IR-CCD imager.

Table 2.
Photomask Sequence for the Self-Aligned IR-CCD Process

Mask Level	Function
M1	Boron p-barrier (channel stop) implant
M2	Buried channel-1
M3	p^+ diffusion
M4	Field oxide
M5	Buried channel-2
M6	Polysilicon 1
M7	Polysilicon 2
M8	n^+ guard rings
M9	n^+ diffusions
M10	Contacts (except SBD contacts)
M11	SBD contacts
M12	SBD dielectric
M13	Metallization

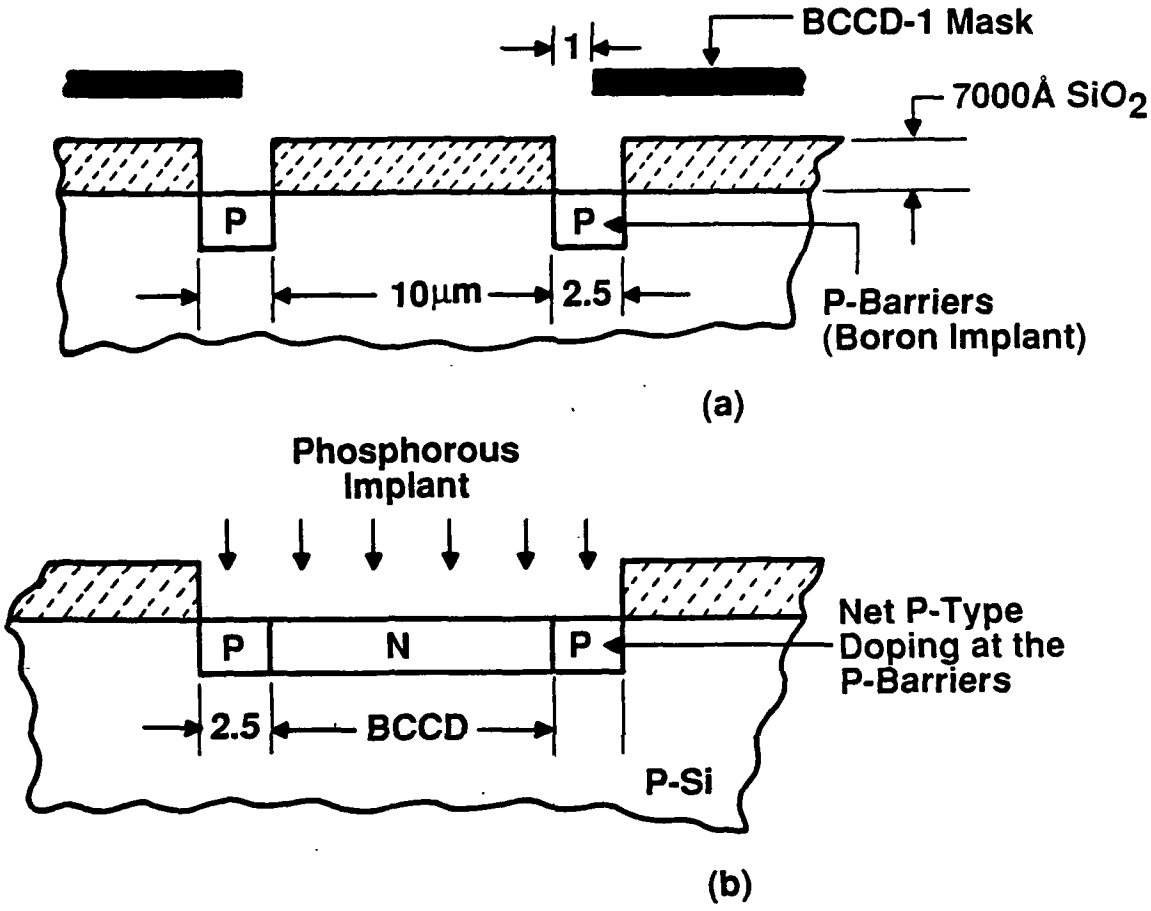

Figure 16. Self-alignment of the p- barrier and the buried-channel CCD implants.

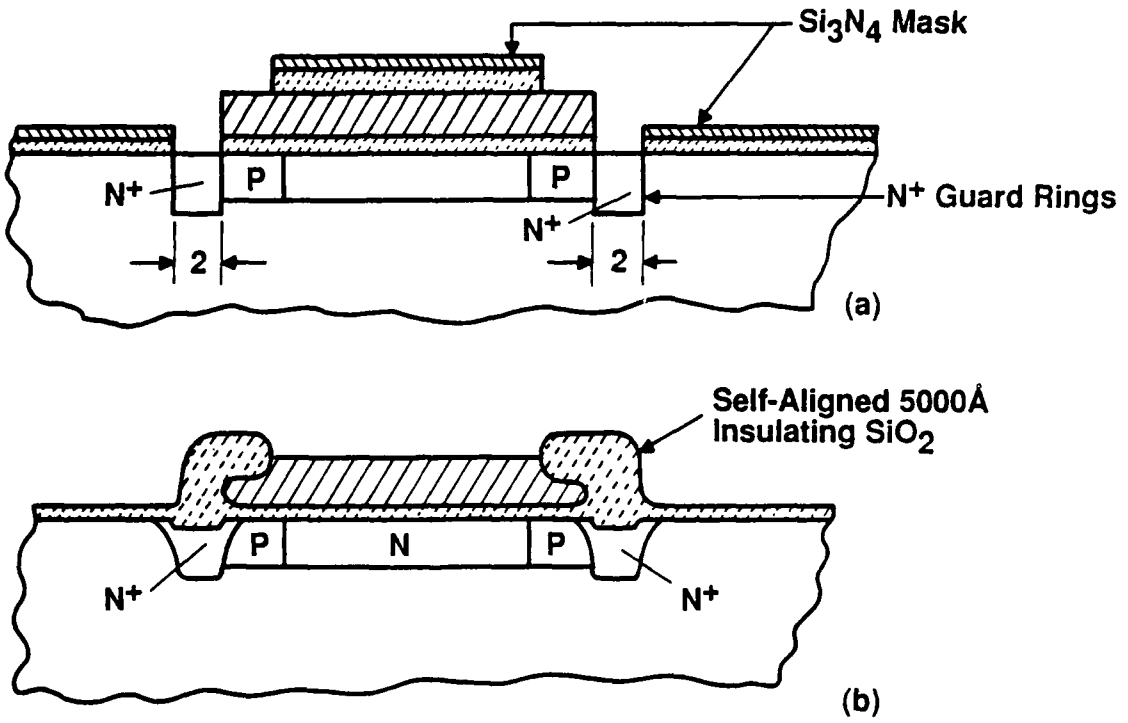

Figure 17. Definition of n+ guard rings and self-aligned insulating oxides.

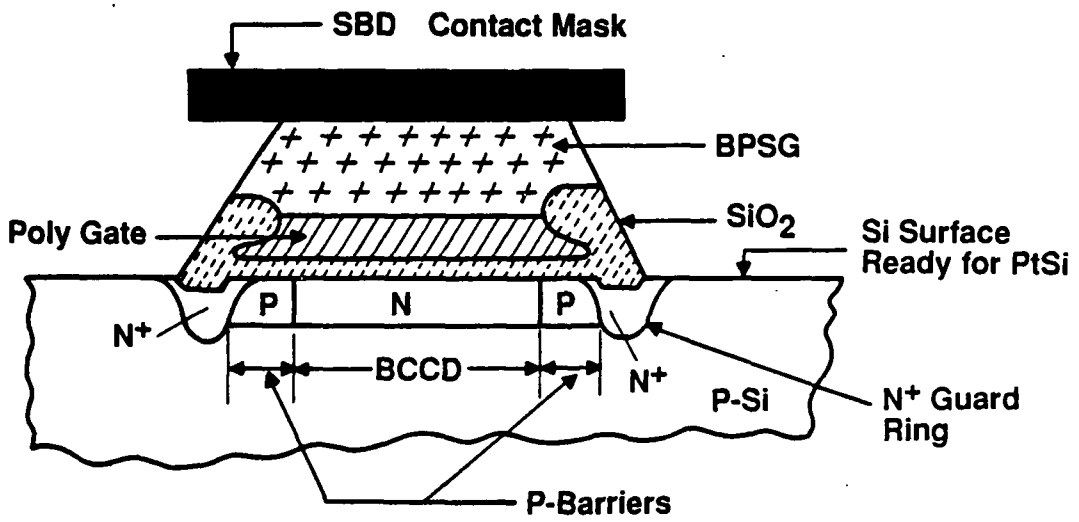

Figure 18. Self-alignment of SBD contacts with n+ guard rings.

2.4.2 Process Simulation

As described in Section 2.3.1, the high-fill-factor design makes use of several self-alignment features, including those for self-alignment of the buried-channel implantation to the p-type channel stops. This process requires that the

initial 7000-Å field oxide be etched first with the boron implant mask, the boron be implanted, and the buried-channel mask be applied to the wafers. The oxide remaining in the buried-channel regions is then etched, and the photoresist is removed. Phosphorus is then implanted to form the buried channels. The p-type channel stops for the buried-channel CCDs, however, are formed by the boron implant that compensates the phosphorus implanted in the channel-stop regions.

To provide an adequate barrier at the edge of the buried channel and to ensure proper blooming control operation for the device, the region having both phosphorus and boron implantations should remain p-type. The maximum boron concentration is limited, however, by breakdown considerations between the boron barriers and the n^+ guard rings.

SUPREM process simulations were run to examine the effect of variations in boron implantation conditions on the net carrier concentrations in the regions of individual and combined boron and phosphorus implantations. These results indicated that the surface was expected to become p-type for total boron implantations above about $1.0 \times 10^{13}cm^{12}$. Figure 19 shows the calculated profile for the net impurity composition after completion of processing in the region having both the buried-channel implantation of $1.3 \times 10^{12}cm^{-2}$ and a total boron-implantation of $1.2 \times 10^{13}cm^{-2}$.* Final implant profiles of boron only and phosphorus only are shown in Figs. 20 and 21, respectively. Discontinuities in the profiles correspond to the polysilicon-to-channel-oxide and channel-oxide-to-bulk-silicon boundaries.

* The total boron implant of $1.2 \times 10^{13}cm^{-3}$ was made as a double implant of $6 \times 10^{12}cm^{-3}$ at 30 keV and $6 \times 10^{-12}cm^{-3}$ at 60 keV.

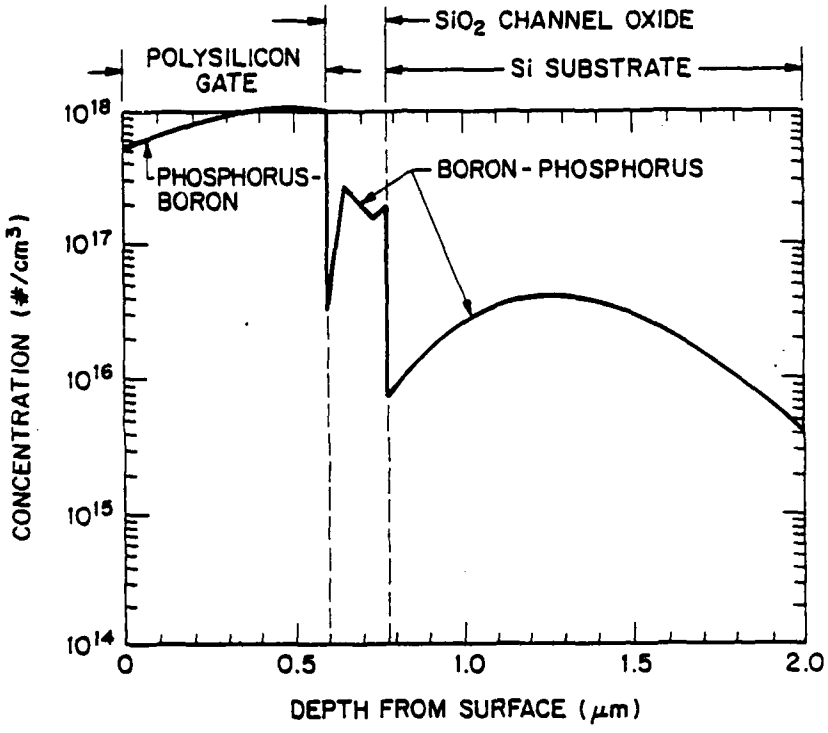

Figure 19. Calculated net impurity concentration profiles for the buried-channel CCD (BCCD) channel-stop regions for BCCD phosphorus implant of $1.3 \times 10^{12} cm^{-2}$ and total boron implant of $1.2 \times 10^{13} cm^{-2}$.

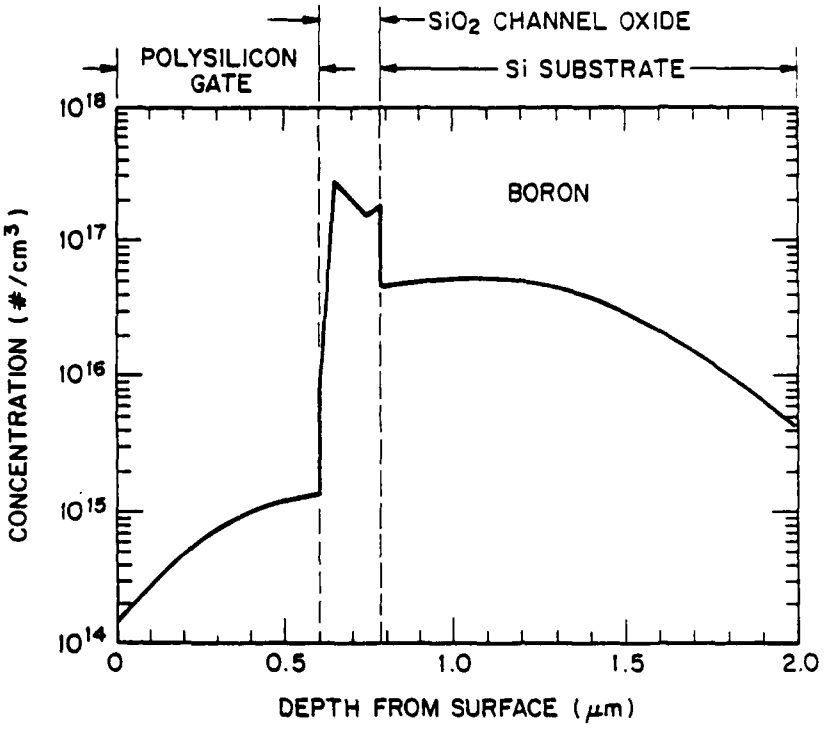

Figure 20. Calculated final boron concentration profile for a total boron implant of $1.2 \times 10^{13} cm^{-3}$.

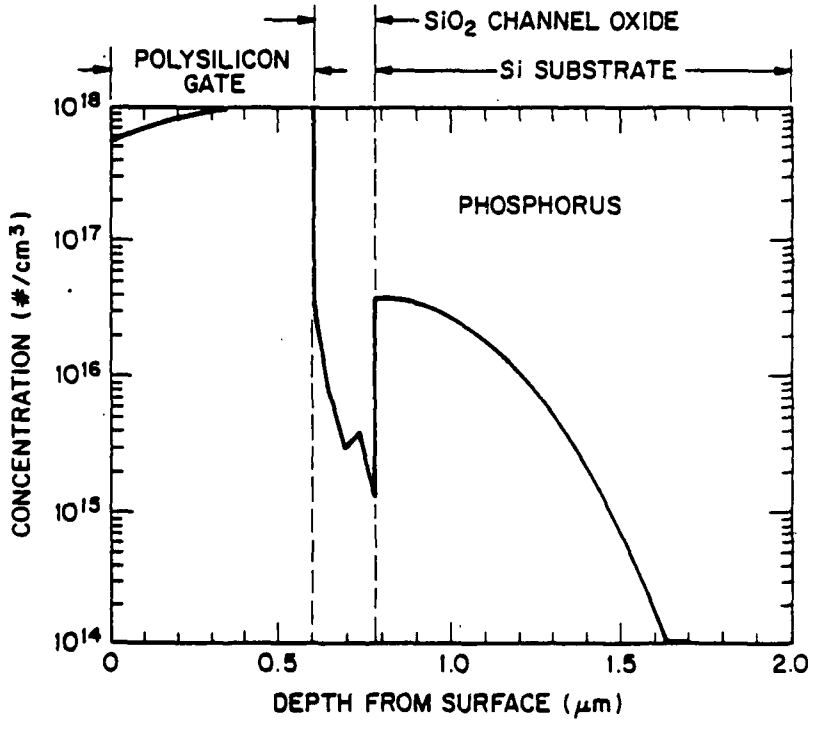

Figure 21. Calculated final phosphorus concentration profile for a phosphorus implant dose of $1.3 \times 10^{12} cm^{-3}$.

2.4.3 Wafer Lots

Because of uncertainties in the exact net surface concentrations of the SUPREM simulations described in Section 2.3.2, a range of boron implantations was used in Wafer Lot No. 1, varying from a total boron dose of 8 x $10^{12}cm^{-2}$ to 15 x $10^{12}cm^{-2}$, as shown in Table 3. In addition to the variation in implantation dosage, Wafer Lot No. 1 was also divided between two types of starting material, namely float-zone (FZ) and magnetically grown Czochralski (MCZ) material. The use of the MCZ material is expected to reduce the amount of swirl-like non-uniformities in the imagers but has not yet been as fully evaluated as the FZ material.

For the fabrication of the Wafer Lot No. 1, we have used a relatively thick (2200 Å) nitride. The removal of this thick nitride by hot H_2So_4-H_3PO_4 on the first ten (10) wafers resulted in excessive etching at the CCD output stage of the polysilicon gates that were exposed to the n^+ diffusion step. As a result of this process failure, the remaining 12 wafers were split two ways. Seven wafers were completed with the guard ring definition and stripping of the nitride by plasma etching before the n^+ diffusion step. For the remaining five wafers, the 2200-Å Si_3N_4 on the SiO_2 layer was removed by wet-etching in hot H_2SO_4-H_3PO_4, and the n^+ guard rings were defined without nitride. In this case, the thicker SiO_2 growth (over the n^+-doped guard rings and the polysilicon gate regions, as compared with the undoped substrate in the SBD regions) was used for the self-alignment of the SBD contacts. Working 160 x 244 and 320 x 244 IR-CCD imagers were obtained from both of these groups.

Table 3.
Wafer Distribution for TA13401A - Lot 1

	Material		Total Boron Implant			
Wafer	FZ	MCZ	8 E12	12 E12	13.5 E12	15 E12
A	x		x			
B	x		x			
C	x		x			
D	x			x		
E	x				x	
F	x				x	
G	x				x	
H	x				x	
I	x					x
J	x					x
K	x					x
L	x			x		
M		x	x			
N		x	x			
O		x	x			
P		x		x		
Q		x			x	
R		x			x	
S		x			x	
T		x		x		
U		x				x
V		x				x
W		x		x		
Totals:	12	11	6	5	7	5

In addition to Wafer Lot No. 1 fabricated under this contract, the David Sarnoff Research Center also processed a Wafer Lot No. 2, funded by another client. In this wafer lot, the boron implant doses were 6, 9, 13, and 15 x 10^{12} cm^{-2}.

The lower boron dose of 6×10^{12} cm^{-2} was introduced because of our concern about high electric fields, at the edges of the n^+ guard rings, leading to potential detector dark-current spikes. Seventeen wafers of the second lot were processed with nitride and five without nitride. For the wafers with nitride processing, the thickness of the nitride was reduced to 250 Å. Plasma-etching was used for the etching of Si_3N_4 and SiO_2 in the guard ring areas, and a wet etch was used to strip the nitride before the n^+ diffusion step. Working IR-CCD imagers were obtained from all 22 wafers of Wafer Lot No. 2.

Both wafer lots were processed with BCCD-1 implant in the form of phosphorus, with a dose of 1.3×10^{12} cm^{-2} and 150 keV. The p^+ diffusions were formed by a boron implant, with a dose of 2×10^{15} cm^{-2} at 35 keV. For the BCCD-2 implant, an arsenic was used, with a dose of 5×10^{11} cm^{-2} at 180 keV. The n^+ guard rings were formed by an arsenic implant, with a dose of 5×10^{15} cm^{-2} at 50 keV, and the n^+ diffusions (for sources and drains) were formed by a phosphorus implant, with a dose of 5×10^{15} cm^{-2} at 50 keV.

The PtSi Schottky-barrier detectors in Wafer Lot No. 1 were fabricated with a nominal thickness of the deposited Pt of 9 Å and were split between anneal times of 3 and 16 h. Wafer Lot No. 2 was completed with a PtSi SBD process consisting of 16-h anneal and was split between 9 and 25 Å of deposited Pt.

Both wafer lots were completed with deposited-SiO_2 SBD cavity dielectric [12, 15, 19] of about 8000 Å and SiO AR coating of 5300 Å.

3.0 OPERATION AND PERFORMANCE

3.1 IR-CCD TV CAMERA TESTER

The performances of the 160 x 244 and 320 x 244 PtSi IR-CCD imagers were evaluated with the IR-TV camera tester shown in Fig. 22 [15, 19]. The IR imagers bonded in the 32-pin ceramic package (see Fig. 11) were cooled to about 77 K by a liquid nitrogen Dewar, shown in Fig. 23. In this test set-up, the camera electronics, including all of the timing and driver circuits, are contained in the enclosure next to the Dewar. The black terminal panel (right side of Fig. 22) contains all of the controls for the camera waveforms and the dc voltages required for operation of the IR-CCD imager. The electronics box to the right of the IR-CCD camera is an off-set-type, one-point response uniformity corrector.* This uniformity corrector forms a reference frame (that is subtracted from each video signal frame) by averaging up to 16 background-exposure frames. The block diagram of the uniformity corrector is shown in Fig. 24. This uniformity corrector, however, was designed for operation with a maximum frame size of 256 x 256 pixels. Therefore, it cannot process the complete frame of the 320 x 244 imager.

The 160 x 244 and 320 x 244 imagers were operated with a standard TV monitor without a frame converter, with the video output corresponding to every second line of standard TV output. To accomplish this, the IR-TV camera test set-up was operated with thirty 160- x 244-element or 320- x 244-element frames/s and two vertically interlaced 160- x 122-element (or 320- x 122-element) fields/frame. This operation produces a video output with a horizontal-line time of 63.5 μs and an imager-output signal, at every second horizontal line, that can be displayed on a standard TV monitor. The total video frame time (including the vertical blanking time) corresponds to two identical (un-interlaced) fields, each with 263 (or 262-1/2)horizontal TV lines.†

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* The same type of one-point uniformity corrector was first reported by W. S. Ewing, of Rome Air Development Center, Hanscom AFB, MA [25].

† Two modes of operation are available. The video time frame with 263 TV lines/field displays a perfect interlace on a standard TV screen, but each frame contains one extra TV line. While RS170 equivalent video output is obtained for the case with 262-1/2 TV lines, this mode of operation results in pseudo-interlace, with pairing of two adjacent lines.

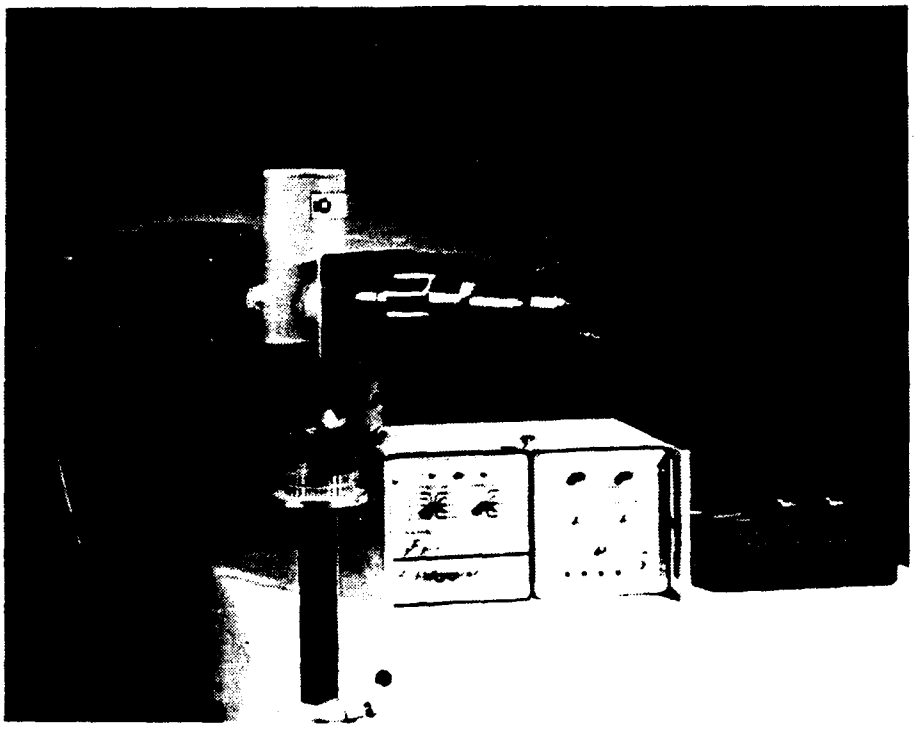


Figure 22. IR-CCD TV camera test set-up.

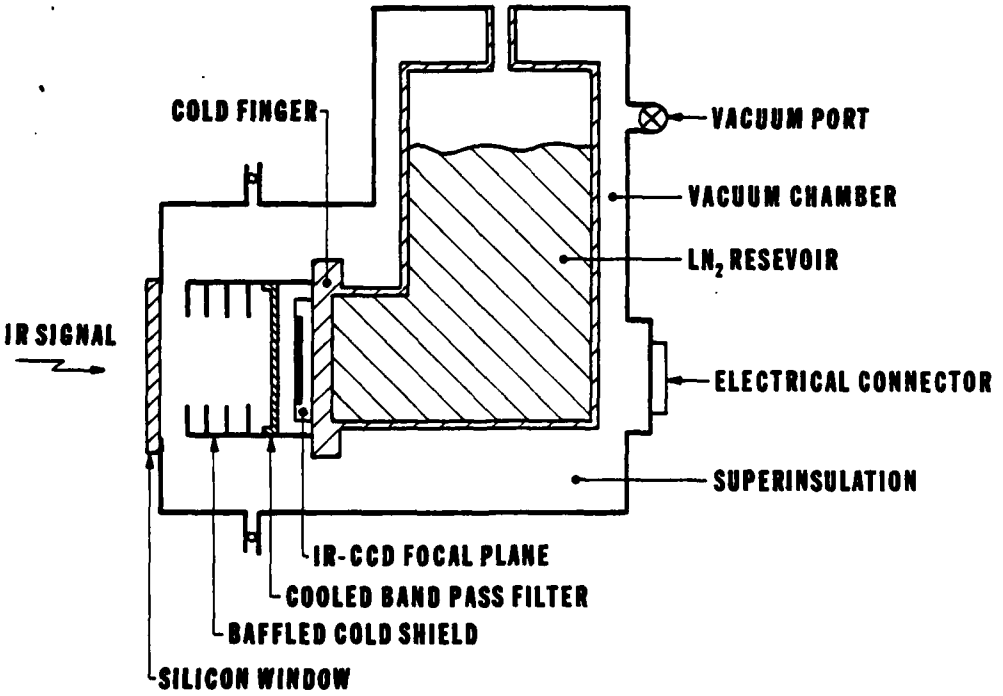


Figure 23. IR-CCD LN Dewar and cold-shield assembly.

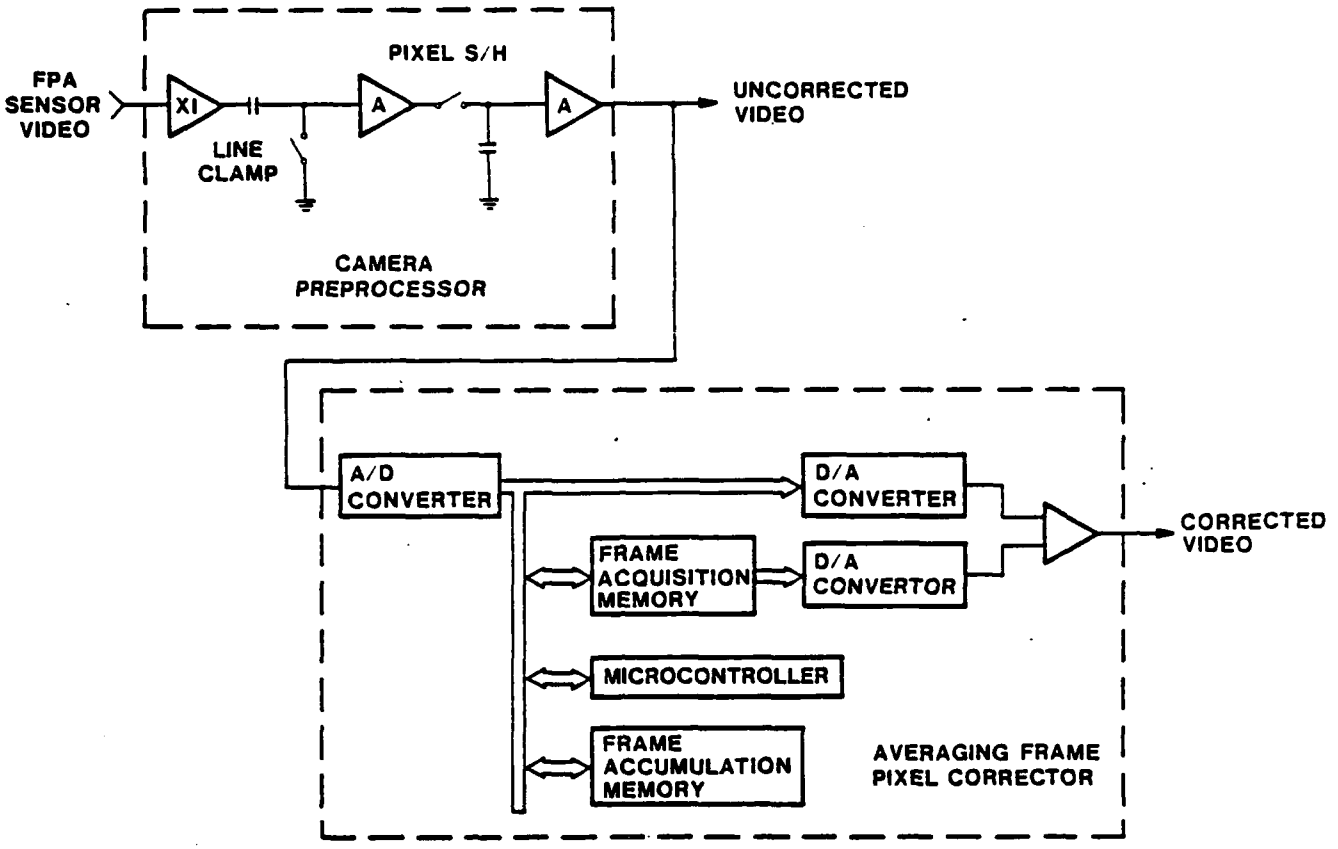


Figure 24. Block diagram of frame-averaging, additive-type, one-point response uniformity corrector.

During the readout of the 160- x 244-element imager frame, the odd field contains the imager readout of the 122 odd lines (i.e., lines 1, 3, 5, ... 243), and the even field contains signals from the 122 even lines (i.e., lines 0, 2, 4, ... 242).

The clock waveforms for the horizontal-line readout of the 160- x 244-element and the 320- x 244-element IR-CCD imagers are illustrated again in Figs. 25 and 26, respectively. During the horizontal-blanking time, T_{HB} = 11.9 μs, the charge stored in the vertical-column B register is moved down one stage by clock phases $\emptyset_{1B}$, $\emptyset_{2B}$, $\emptyset_{3B}$, and $\emptyset_{4B}$, and the charge signal is transferred from the last stage of the parallel B register to the series-output C register by clock phases $\emptyset_{4B}$, $\emptyset_{1C}$, and $\emptyset_{4C}$.

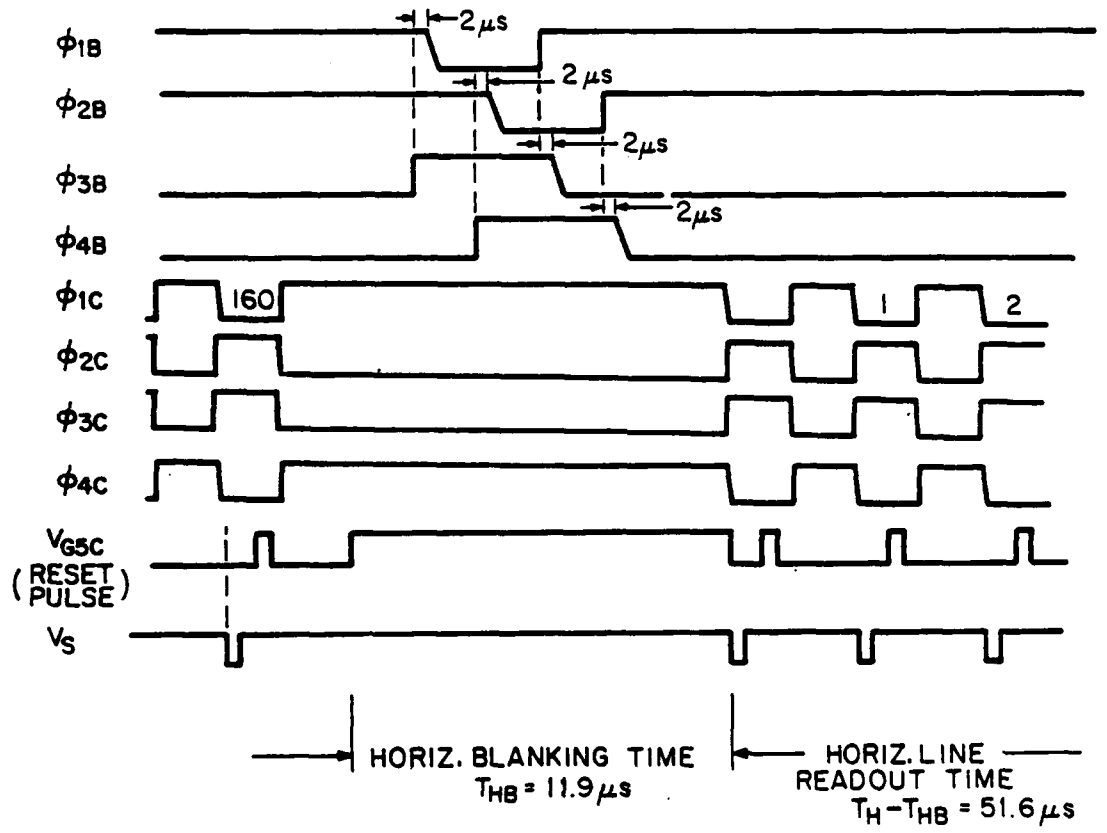


Figure 25. Waveforms for horizontal-line readout of the 160- x 244-element IR-CCD imager.

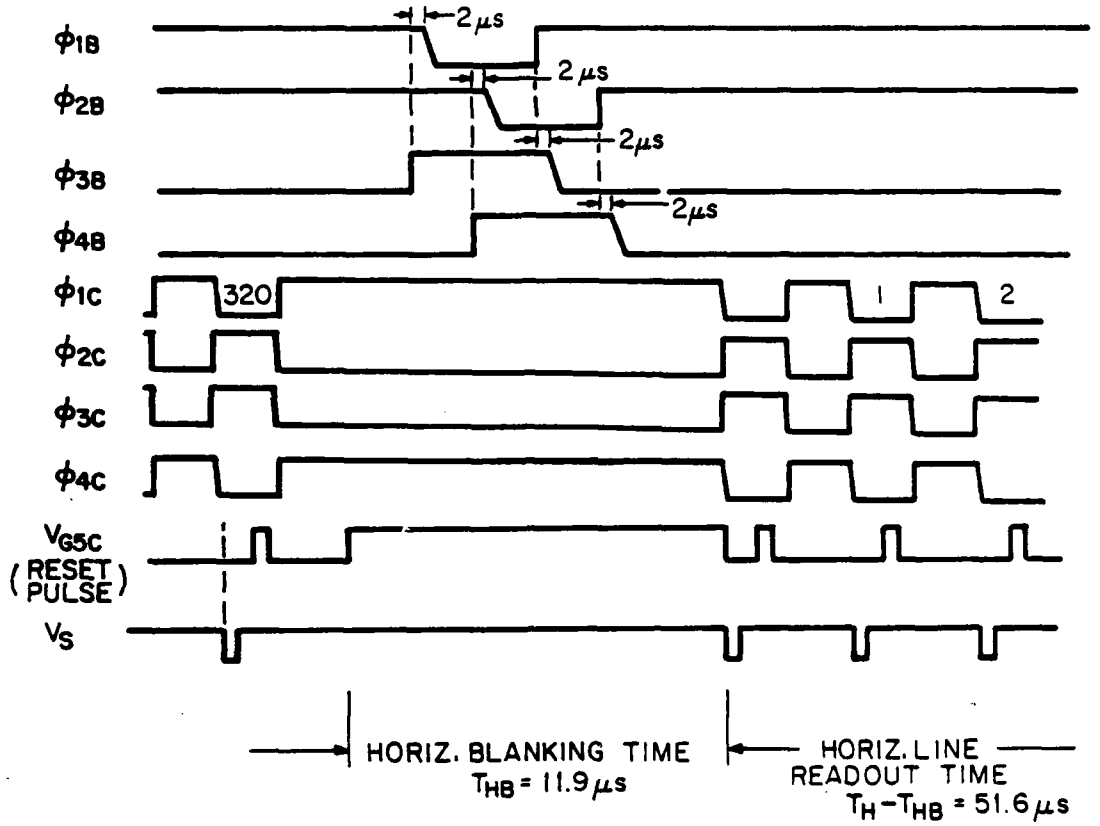


Figure 26. Waveforms for horizontal-line readout of the 320- x 244-element IR-CCD imager.

At this point, it should be mentioned that the new 160 x 244 and 320 x 244 IR-CCD imagers were originally designed for operation with a 4-phase double-clock that operates with potential wells extending over two and three gates. We have found, however, that much lower charge-transfer losses (charge-transfer inefficiency) can be achieved for the new 160 x 244 and 320 x 244 IR-CCD imagers by operating the serial-output C register with a symmetrical 2-phase clock [28, 29]. Because of the available gate structure of the C registers, the performance of these arrays was tested by operating the C register with a 2-phase clock using polysilicon-2 gates with $Ø_{1C}$ and $Ø_{3C}$ clocks as the storage gates, and the polysilicon-1 gates with $Ø_{4C}$ and $Ø_{2C}$ clocks as the barrier gates. The clock waveforms for operation of the C register are illustrated in Fig. 27. Figure 28 illustrates the operation of the input stage in the fill-and-spill mode [27], and Fig. 29 illustrates the operation of the floating-diffusion output stage.

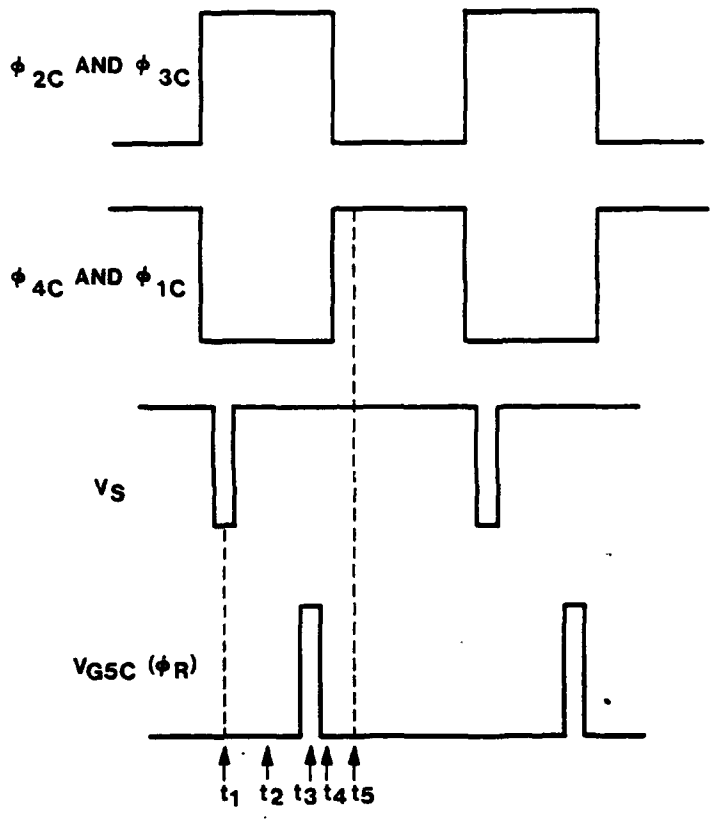


Figure 27. Waveforms for operation of the serial output C register (see Figs. 28 and 29) with a 2-phase symmetric clock.

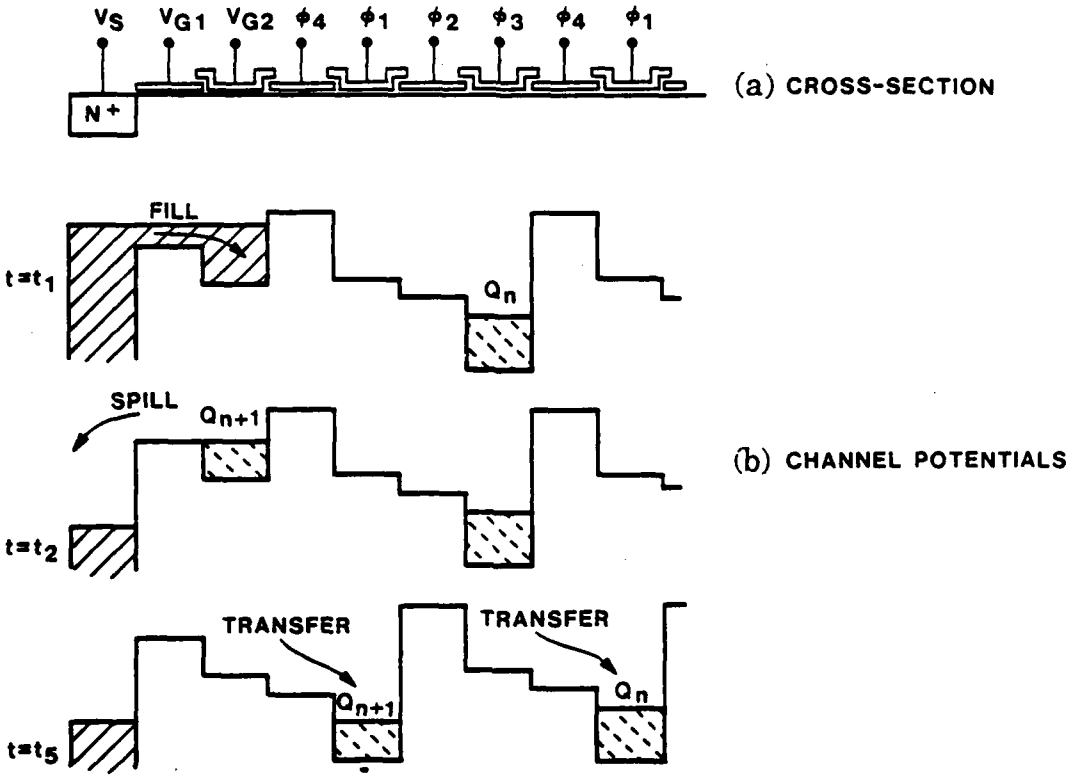


Figure 28. Operation of the C register input stage in fill-and-spill mode showing the clocking of the input gate structure in (a) and the channel potentials for operation in (b).

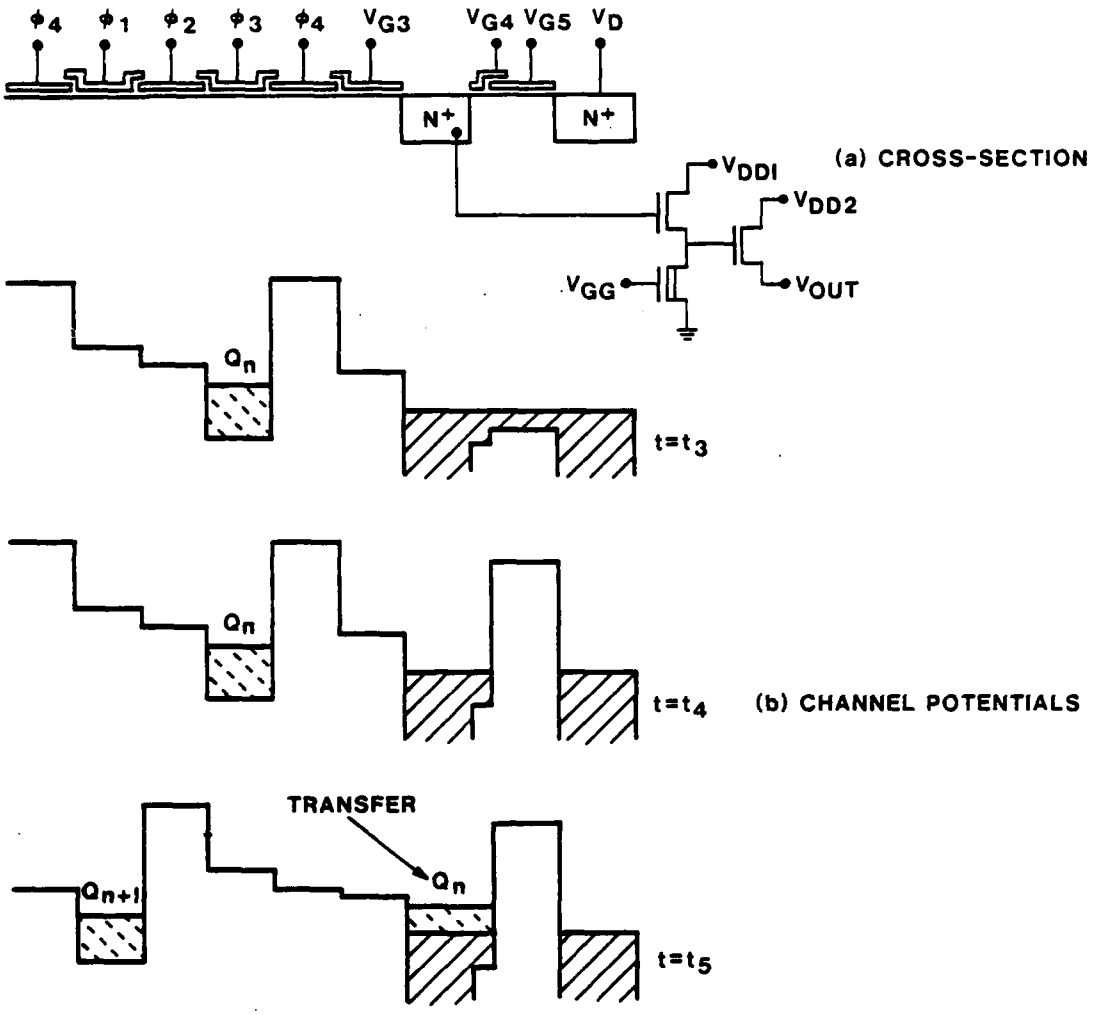


Figure 29. Operation of the C register output stage showing the clocking of the input gate structure in (a) and the channel potentials for operation in (b).

The waveforms for the horizontal and vertical syncs and the B clocks are shown in Fig. 30. The readout of each frame is controlled by a train of 526 horizontal-blanking pulses, each corresponding to a standard TV line time of 63.5 μs. The horizontal-blanking signal is obtained from a television sync-generator IC (TA6993W). As shown in Fig. 30, each field time consists of 263 standard TV lines (each 63.5 μs in duration), and the frame time corresponds to 526 TV line times. The imager B clock readout, however, is controlled by the 1/2-horizontal-blanking signal and the vertical-blanking signal that produce two interlaced output fields, each with 122 output video lines, with each 63.5-μs output video line separated by an empty 63.5-μs line time. The end of the readout of the odd field

(lines 1, 3, 5, ... 243) and the beginning of the readout of the even field (lines 0, 2, 4, ... 242) are illustrated in Fig. 30 (a).

The transition from the even-frame to the odd-frame readout is illustrated in Fig. 30 (b). This mode of readout, with 526 (rather than the standard 525) 63.5-μs TV lines/frame, permits the display on a standard TV monitor of two properly interlaced 122-line fields without the use of a field or frame buffer. The penalty of this simplified readout system is that only one-half of the TV display lines contain the video signal, and there is one extra TV line time/frame as compared with the standard TV signal.

Figure 30 also illustrates the parallel-column register (B) clocks ($\emptyset_{1B}$, $\emptyset_{2B}$, $\emptyset_{3B}$, and $\emptyset_{4B}$) for both interlaced fields. During the blanking time (corresponding to 19 63.5-μs TV lines) preceding the odd-field readout (Fig. 30 b), the charge signal detected in the odd-field SBDs is transferred from the SBDs to the parallel-column registers under the $\emptyset_{1B}$ and $\emptyset_{2B}$ gates. This is accomplished by applying a positive voltage pulse, V_{BT-1}, to the $\emptyset_{1B}$ gates. A surface part of the $\emptyset_{1B}$ (as well as $\emptyset_{3B}$) gate acts as the transfer gate between the SBD and the BCCD register. Therefore, a net positive voltage applied to the $\emptyset_{1B}$ gate is required to form a transfer channel between the SBDs and the BCCD register. However, for storing and transferring of the original charge in the parallel register, the B clocks ($\emptyset_{1B}$, $\emptyset_{2B}$, $\emptyset_{3B}$, and $\emptyset_{4B}$) switch between two negative voltages only (Fig. 15).

The readout of the signal charge, detected by the even-field SBDs [Fig. 30 (a)], is similar except that the $\emptyset_{3B}$ gate performs the function of the transfer gate. During this transfer, the $\emptyset_{2B}$ clock is also in a high-voltage state, while the $\emptyset_{1B}$ and $\emptyset_{4B}$ clocks are in a low-voltage state. As shown by the B-clock waveforms in Fig. 30, at the end of the vertical-blanking time preceding either the odd- or the even-field readout, the charge for either field is at the same location of the parallel register, i.e., under the $\emptyset_{1B}$ and $\emptyset_{2B}$ gates.

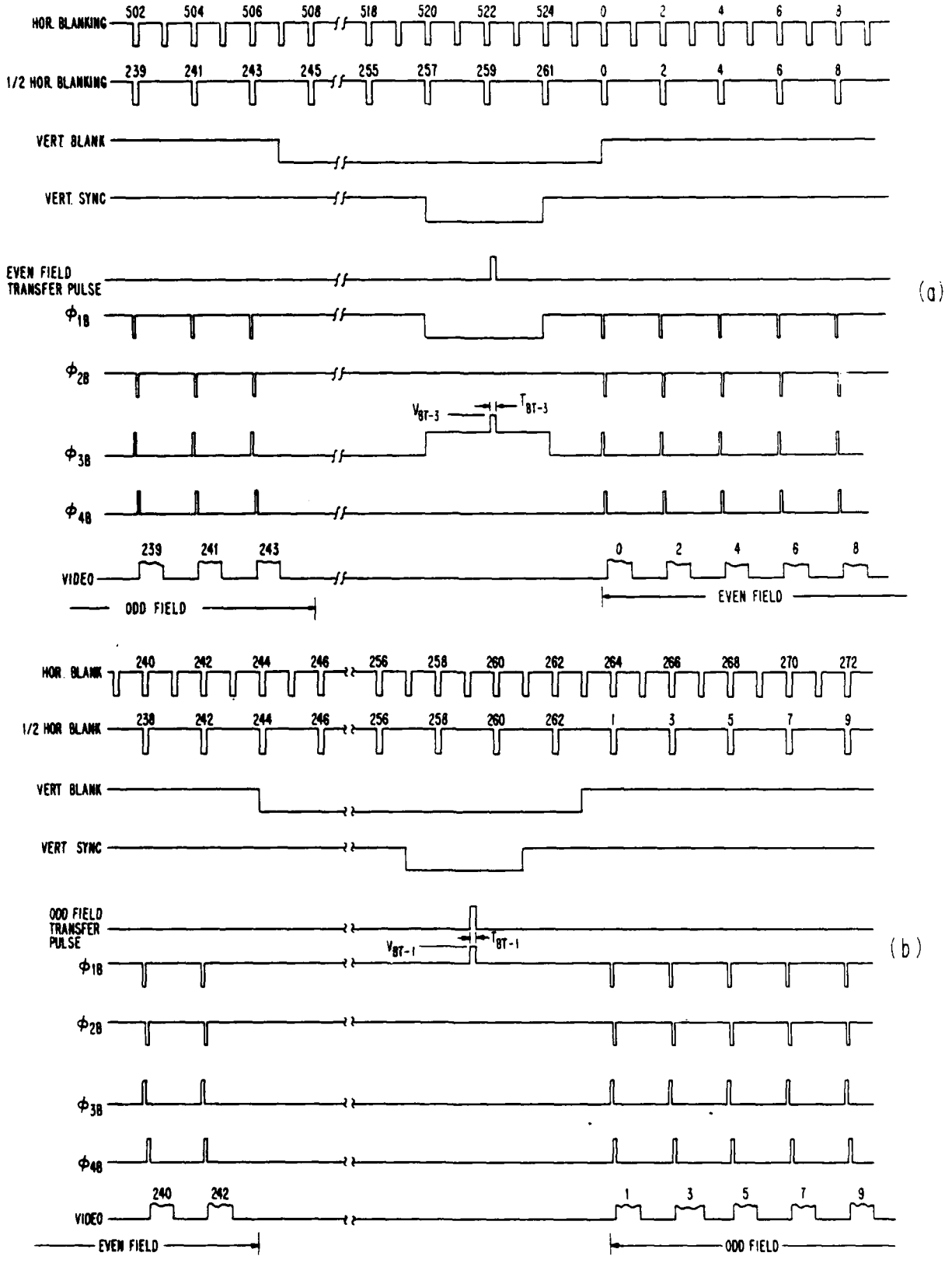


Figure 30. Waveforms of horizontal and vertical sync and B clock for the 160 x 244 and 320 x 244 IR-CCD imagers operating with a 2:1 vertical interlace.

The waveform generator for operating the IR-CCD imagers was built to provide sufficient flexibility to optimize the operation of the arrays. Therefore, each individual clock pulse, such as G_{3C} and G_{5C}, has a separate dc level and amplitude control. The clock phases for the A, B, and C registers were provided with amplitude control for the $\emptyset_A$, $\emptyset_B$, and $\emptyset_C$ clocks and with a separate dc-level control for the respective polysilicon-1 and polysilicon-2 gates, i.e., $\emptyset_{1\text{-}3A}$, $\emptyset_{2\text{-}4A}$, $\emptyset_{1\text{-}3B}$, $\emptyset_{2\text{-}4B}$, $\emptyset_{1\text{-}3C}$, and $\emptyset_{2\text{-}4C}$. The separate voltage controls for operation of the 160-element x 244-element IR-CCD imagers are listed in Table 3. Typical values of the above pulses used for the operation of the arrays are listed in Table 4. It should be noted that to obtain an independent control for the B clock CCD-transfer voltages and the reset-bias voltage of the SBDs, the $V_{BT\text{-}1}$ and $V_{BT\text{-}3}$ voltage levels can be adjusted independently of the $\emptyset_{1B}$ and $\emptyset_{3B}$ dc bias and amplitude.

Table 4.
Separate Voltage Controls for Operating the IR-CCD Imagers

Voltage Controls	DC Voltage Levels (V)	Voltage Pulses (V)
Source-Drain Diffusions V_{SA}, V_{SC}, V_{DA}, V_{DC}, V_{DD1}, V_{DD2}, and V_{SO}	0 to +15	---
DC-Biased Gates: G_{1A}, G_{2A}, G_{1C}, G_{2C}, G_{3C}, G_{4C}, G_{5C}, and V_{GG}	-15 to +15	---
Serial Clocks: $\emptyset_{1A}$, $\emptyset_{2A}$, $\emptyset_{3A}$, $\emptyset_{4A}$, $\emptyset_{1C}$, $\emptyset_{2C}$, $\emptyset_{3C}$, and $\emptyset_{4C}$	-15 to +15 (base)	0 to +15 (amplitude)
Parallel Clocks: $\emptyset_{1B}$, $\emptyset_{2B}$, $\emptyset_{3B}$, and $\emptyset_{4B}$	-15 to 0 (base)	0 to +15 (amplitude)
$V_{BT\text{-}1}$ and $V_{BT\text{-}3}$	0 (base)	0 to +15 (peak)

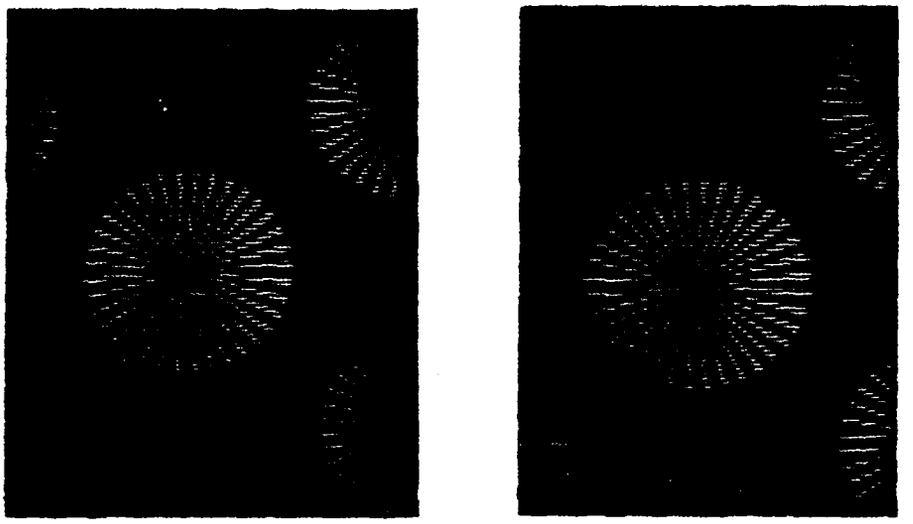
3.2 EXPERIMENTAL RESULTS

3.2.1 Operation of 160 x 244 and 320 x 244 IR-CCD Imagers

The operation of the high-fill-factor 160 x 244 IR-CCD imager (TA13401A) was tested in the IR TV camera set-up (described in Section 3.1) that was originally developed for operation of the 160 x 244 TA11524 imagers. The initial operation of the 320 x 244 imager was demonstrated by operating this imager with a 3.1-MHz horizontal clock. However, further testing of the 320 x 244 imagers revealed a very good charge transfer efficiency for a horizontal clock of 6.2 MHz. This allows display of the 320 x 244 imager directly on a standard TV monitor, without the need of a frame converter.

The comparison of the resolutions of the 160- x 244-element imager and the 320- x 244-element imager is illustrated in Fig. 31. For the test illustrated in this figure, both imagers were operated with a 3.1-MHz C register clock, which allows the display of only one half of the detected image of the 320 x 244 imager. The imaging of the same test pattern by the 320 x 244 array operating at 6.2 MHz is shown in Fig. 32. The main improvement in performance observed for the high-fill-factor 160 x 244 imagers and the 320 x 244 imagers was a more uniform response and striation-free image for the case of the devices made on MCZ wafers. Due to vertical aluminum busses for the B clock, these imagers also showed very uniform onset of response for operation with low SBD operating voltages.

The main shortcoming observed in the operation of the new 160 x 244 and the 320 x 244 imagers is the presence of SBD dark-current spots that tended to increase in number as the SBD bias voltage increased above 2 to 3 V (determined by the values of V_{BT} as shown in Figs. 15 and 30. The presence of these dark-current spots, with the corresponding SBD responsivity and (full-well) saturation signal, is illustrated in Fig. 33 for the best-quality devices tested.



160 X 244
(40 X 80 μm pixels)

320 X 244
(40 X 40 μm pixels)

Figure 31. Comparison of resolution for 160 x 244 and 320 x 244 PtSi IR-CCD imagers operating with a horizontal clock of 3.1 MHz.

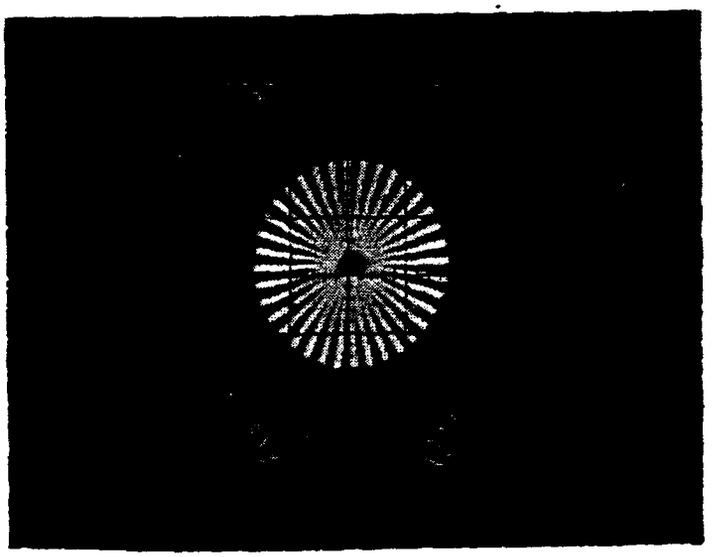
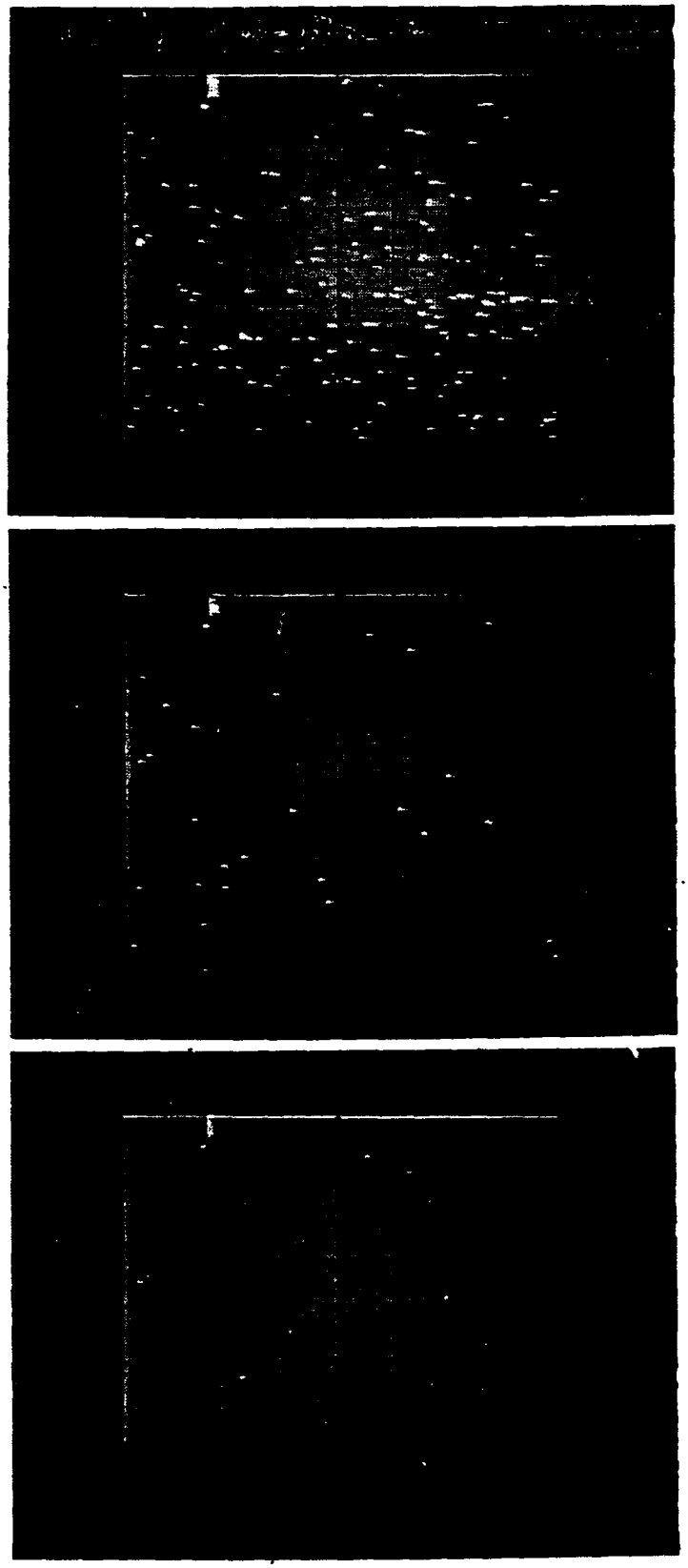


Figure 32. Imaging of test pattern by 320 x 244 PtSi IR-CCD FPA for operation with a horizontal clock of 4.7 MHz.



(a) $R = 3.7 \times 10^4$ elec/pixel/°C
Full Well = 2.6×10^6 elec/pixel

(b) $R = 3.3 \times 10^4$ elec/pixel/°C
Full Well = 1.5×10^6 elec/pixel

(c) $R = 3.0 \times 10^4$ elec/pixel/°C
Full Well = 1.07×10^6 elec/pixel

Figure 33. Dark-current spots, saturation signal (FW), and responsivity for high-fill-factor 160 x 244 imager TA13401A-2S-23 as the SBD bias voltage is increased from (a) to (c) for operation at 30 frames/s, f/2.35 cold shield, and 3.4-μm long-pass-filter.

A preliminary study of a number of new 160 x 244 and 320 x 244 imagers indicated that the maximum useful SBD operating voltage for most imagers was in the range of from 1.5 to 3.0 V. Previously made 160 x 244 IR-CCD imagers, with 39% fill factor, and implanted n-type or n^+ guard rings in the form of phosphorus, did not exhibit these types of dark-current spikes. However, the same 160 x 244 imagers, with 39% fill factor, made by a silicon foundry that we are working with (also with arsenic n^+ guard rings), showed similar dark-current spots, even without the PtSi deposition step. Therefore, we attribute the presence of the observed dark-current spots to high electric fields associated with the n^+ arsenic guard rings that tend to activate material defects in the silicon substrate. Consequently, the dark-current spots are expected to be eliminated by modification of the process, which will result in n type guard rings with more graded impurity profiles.

3.2.2 Performance Characteristics of 160 x 244 and 320 x 244 IR-CCD Imagers

3.2.2.1 Saturation Signal

Direct measurement of C register drain current showed that the new 160 x 244 IR-CCD images with a 10-μm-wide B register channel, is capable of a saturation signal (F.W.) of 2.6×10^6 electrons/pixel. This data suggests that BCCD channels of the B register have a charge handling capacity of 6,500 electrons/μm^2. This increased value over the previously reported value of 3,500 electrons/μm^2, [15, 19] is attributed to more uniform clock voltages of the parallel B register caused by the introduction of the vertical aluminum busses.

The maximum measured saturation signal for the 320 x 244 imager was about 1.5×10^6 electrons/pixel. Since the vertical column register in this device was designed to be 7-μm-wide, a somewhat higher saturation signal is expected for the case of charge-handling capacity of 6500 electrons/μm^2.

3.2.2.2 FPA Responsivity

Based on the measurement of the C register drain current, 160 x 244 images with 80-μm x 40-μm pixels and 60% nominal fill factor have responsivity in the range of from 3.0 to 3.7×10^4 electrons/pixel/°C, depending on the SBD operating voltage (see Fig. 33). This data corresponds to operation with 30 frames/s, f/2.35 optics, and 3.4-μm long-pass filter.

The responsivity of several 320 x 244 imagers was measured to be 8.8 x 10^3 electrons/pixel/°C for f/2.0 optics and 1.3 x 10^4 electrons/pixel/°C for f/2.35 optics.

3.2.2.3 Noise Equivalent Temperature (NEΔT)

A test of 160 x 244 imagers, with a 60% fill factor and operating with f/2.35 cold shield, gave a readout noise of 1000 rms electrons/pixel, responsivity of 2.5 x 10^4 electrons/pixel/°C, and the resulting noise equivalent temperature (NEΔT) of 0.04°C. Since the measured 300 K background for this imager was about 7 x 10^5 electrons, the measured readout noise was larger than the shot-noise-limited value. Furthermore, as the imager background was reduced, a considerably higher readout noise than shot noise was observed.

The noise measurements of a 320 x 244 imager for f/2.0 cold shield gave a readout noise of 500 rms electrons/pixel for the 300 K background of 2.5 x 10^5 electrons/pixel and FPA responsivity of 1.3 x 10^4 electrons/pixel/°C. Based on the above data, this FPA also had a shot-noise-limited performance with an NEΔT of 0.038°C. For lower background signals, the tested 320 x 244 imager exhibited readout noise larger than shot noise. However, for background signals above 2.5 x 10^5 electrons/pixel, the readout noise appears to decrease below 400 rms electrons/pixel as the background signal was increased to 5 x 10^5 electrons/pixel.*

Our previous measurements for readout noise for IR-CCD imagers with PtSi SBDs indicate that readout noise depends on the SBD process, and imagers that have a larger SBD dark current tend to have excess readout noise. Therefore, an SBD process that has a very low dark current, or operation at a temperature of less than 77 K, is needed to achieve SBD imagers that have very low readout noise.

3.2.2.4 SBD Characteristics

The best responsivity and dark-current characteristics of our Schottky-barrier detectors are illustrated in Figs. 34 and 35 for our SBD process with 9 Å of Pt and 16-h anneal. The SBD responsivity characterized by a C_1 coefficient of 0.26 eV^{-1} and Ψ_{ms} of 0.219 eV has been obtained by a large (2.5 x 10^5 μm^2) test detector operating at 4-V bias. The measured SBD responsivities obtained for test diodes along the perimeter of the 320 x 244 imagers correspond to C_1 coefficients in the

* Somewhat similar data was also observed by W. Ewing from RADC, Hanscom AFB for these FPAs [30].

range of from 0.18 to 0.28 eV^{-1}, with the Ψ_{ms} values being less variable. An extensive study of the SBD responsivities was not included in this program, but our data suggests that the responsivities measured for the SBDs of the FPAs are 10% to 20% smaller than those for large test SBDs. This can be explained by the fact that the actual size of the active SBD area apparently is 1.0 to 2.0 μm smaller (on each side) than the nominal inside dimension of the n^+ guard rings. Our data also suggests that the thickness of the dielectric of SBD elements of the imager is not as uniform across the array as it is across the large test diode.

3.2.2.5 Transconduction Gain and Floating Diffusion Capacitance

The transconduction gain of 350 electrons/mV or 2.8 μV/electron was measured for the two-stage, source-follower, C register output amplifier for operation with a 5-kΩ off-chip load restore. This measurement represents an average value computed from a ratio of $\Delta V_{out}/\Delta I_D$ for a number of pixels of a 320 x 244 imager.

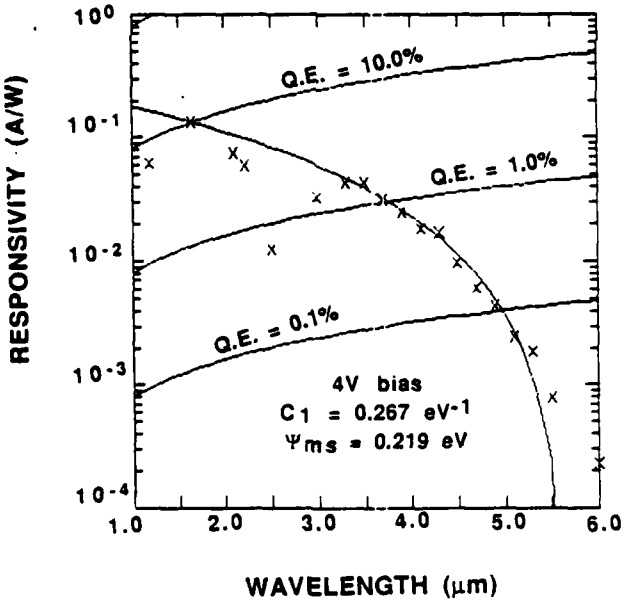


Figure 34. Responsivity of PtSi Schottky-Barrier detectors.

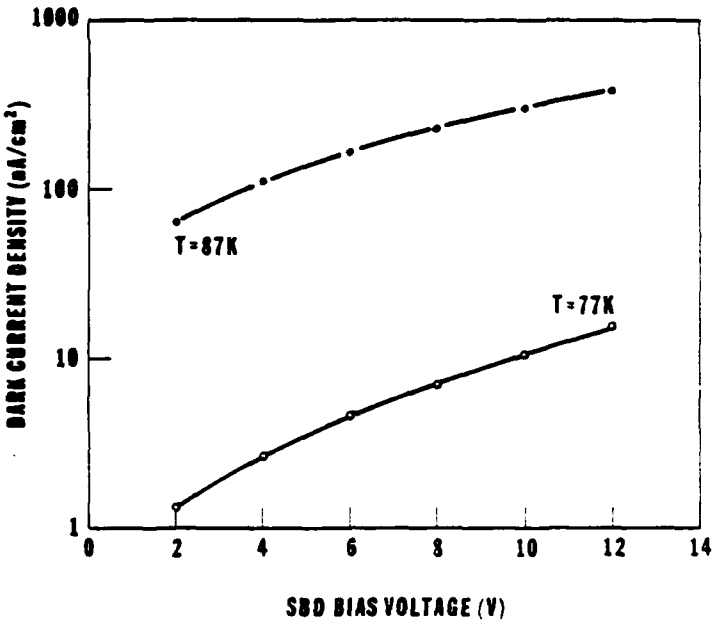


Figure 35. Dark-current density vs bias voltage for PtSi SBDs.

The voltage gain between the floating diffusion node and the output was measured as 0.8. Using this value and the measured transconduction gain of 350 electrons/mV, the measured value of the floating diffusion capacitance is 0.045 pF. This should be compared with the estimated value from the layout of 0.04 pF.

3.2.3 Charge Transfer Inefficiency of C Register

Very low charge-transfer inefficiency (loss) was measured for operation of the C register of the 320 x 244 imager. The data for these measurements at 77 K, with a 2-phase 3.1-MHz clock, as a function of signal charge for several values of bias charge (fat zero) is shown in Fig. 36. A waveform of an output signal for these tests is shown in Fig. 37. For this test, the signal charge is 1.4×10^5 electrons/pixel, the background charge is 3.5×10^4 electrons/s, and the charge-transfer inefficiency is 1.2×10^{-4}/transfer.

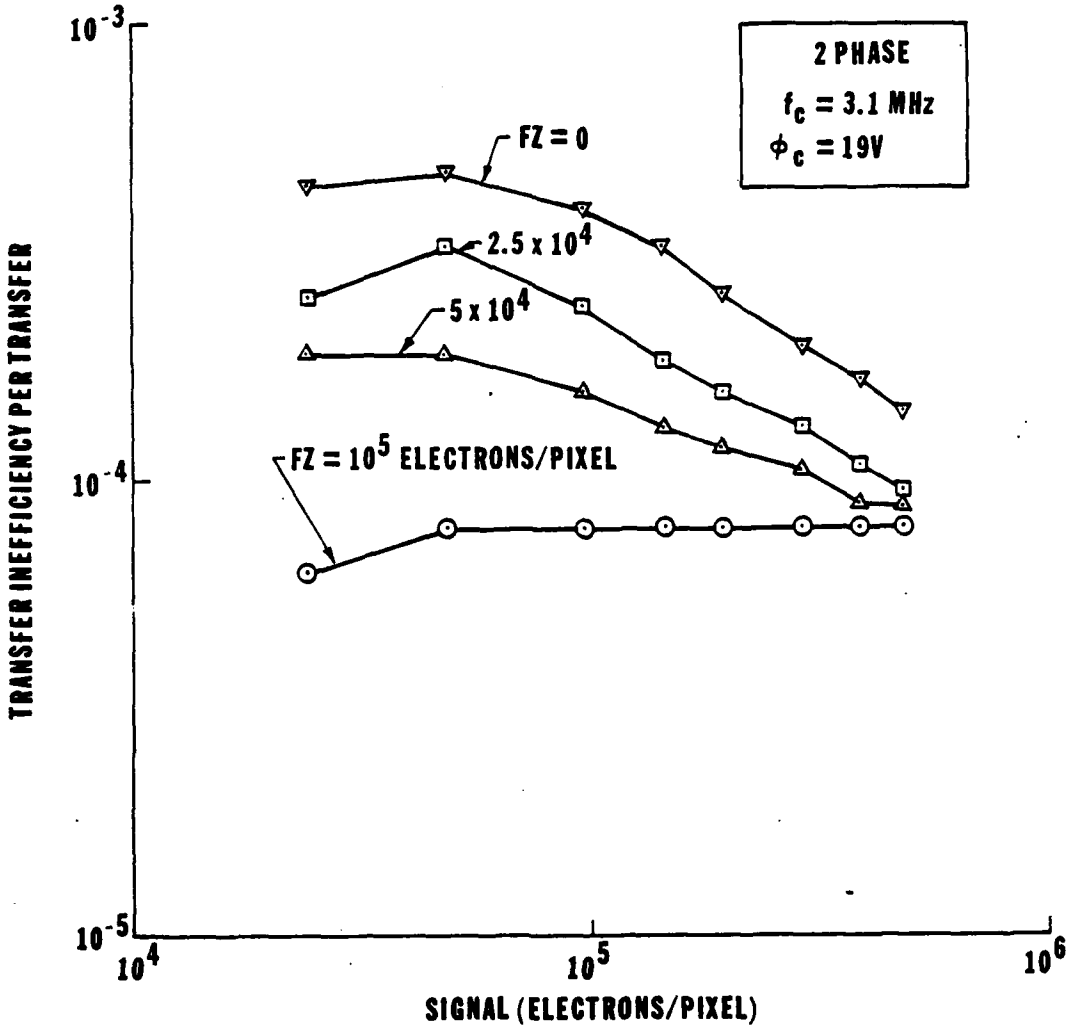


Figure 36. Charge transfer inefficiency of the C register of the 320 x 244 imager as function of signal charge, and background charge (fat-zero) at 77 K for 3.1-MHz 2-phase clock.

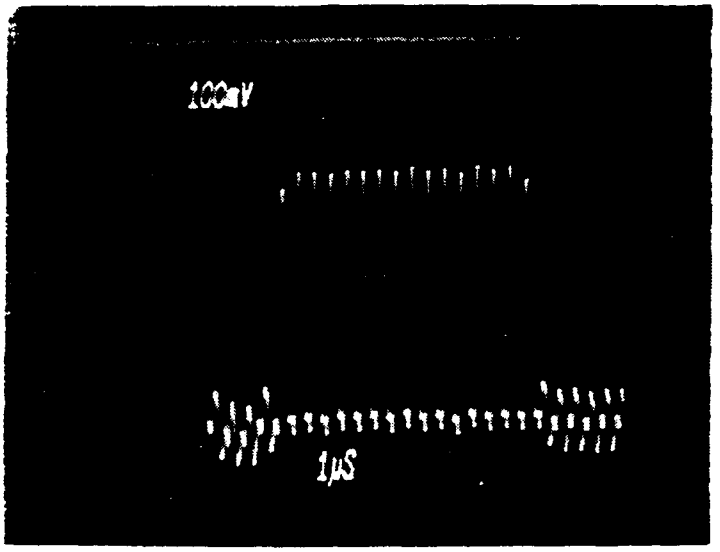
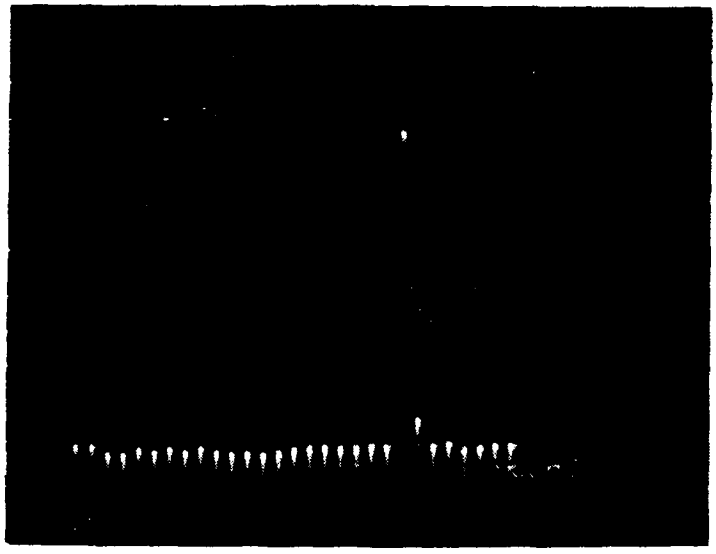


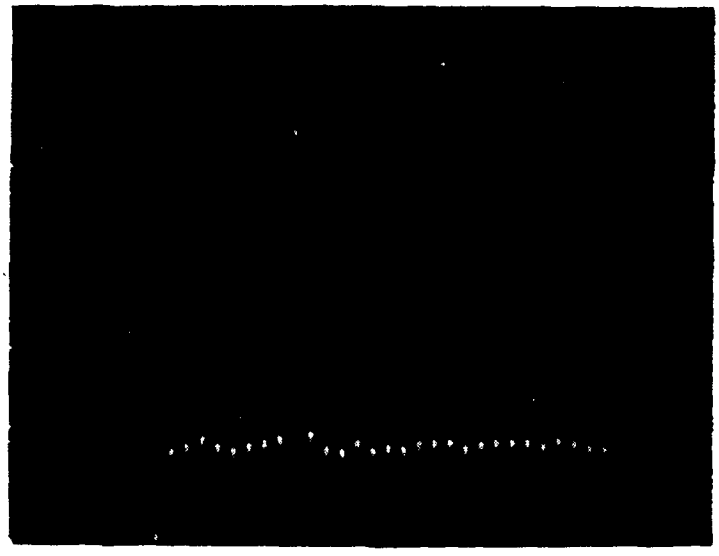
Figure 37. Output waveform of a pulse input to the C register of the 320 x 244 imager operating at 77 K with a 3.1-MHz 2-phase clock.

The performance of the C register of the 320 x 244 array, for operation with a 6.2-MHz horizontal clock for a light spot illuminating a single pixel on both sides of the imager is illustrated in Fig. 38. Comparison of the waveforms in Fig. 38 (a) with those in Fig. 38 (b) shows charge-transfer inefficiency of 7.4×10^{-5} for transfer of a signal charge of 2.2×10^5 electrons/pixel and a background charge of 2.7×10^5 electrons/pixel.

Owing to longer C-register gates (20 μm vs 10 μm) and smaller electric-fringing fields, the 160 x 244 imager exhibited considerably larger charge-transfer inefficiency than the 320 x 244 imager. However, Fig. 39 illustrates that, for typical background signals, the horizontal-transfer inefficiency of the 160 x 244 imager is sufficiently low to result in negligible effect on the horizontal resolution of this imager.



(a)



(b)

Figure 38. Output waveform of a 320 x 244 array operating with the horizontal clock of 6.2 MHz for a light illuminating the imaging area near the output stage in (a) and the opposite in (b).

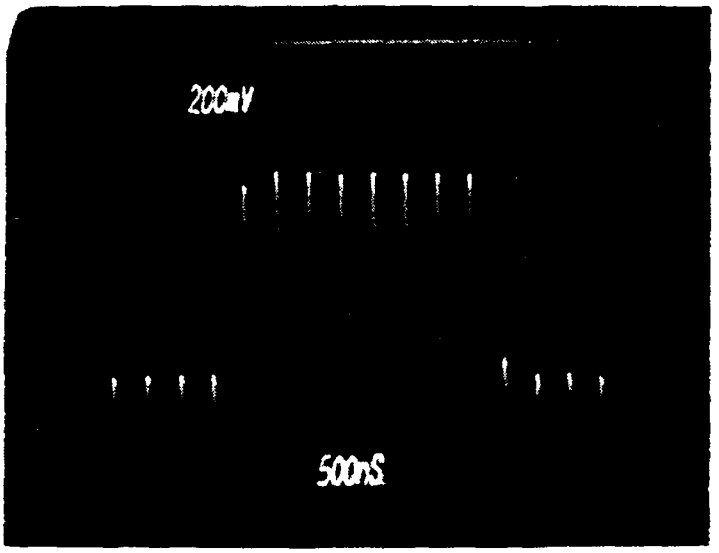


Figure 39. Output waveform for a pulse input to the C register of the 160 x 244 imager for a 3.1-MHz 2-phase clock. The signal charge is 3.5 x 10^5 electrons/pixel, background charge is 2.8 x 10^5 electrons/pixel, and the charge-transfer inefficiency is estimated as 3 x 10^{-4}/transfer.

4.0 CONCLUSIONS

We have succeeded in demonstrating a 160 x 244-element IR-CCD imager that has 80-μm x 40-μm pixels, with a 60% fill factor and a saturation signal of more than 2 x 10^6 electrons/pixels. This imager was fabricated using a Perkin-Elmer 1:1 projection microaligner with minimum features of 2.5-μm and ±1.0-μm alignment tolerances by introducing an IR-CCD process with several self-aligning features.

A 320 x 244-element IR-CCD imager that has 40-μm x 40-μm pixels, a 43% fill factor, and a saturation signal of about 1.5 x 10^6 electrons/pixel was fabricated on the same 4-in. silicon wafer as the 160 x 244 imagers.

The horizontal serial registers of both above imagers were made in the form of a 12-μm-wide, buried-channel CCD, with an additional 3-μm-wide deeper channel to reduce charge-transfer inefficiency for low-level charge signals. Very low charge-transfer inefficiency of 8 x 10^{-5}/transfer was demonstrated for operation of the horizontal output register of the 320 x 244 imager, with 3.1-MHz and 6.2-MHz 2-phase clocks for a wide range of signal charge corresponding to 2.5 x 10^4 to 10^6 electrons/pixel and a relatively low background charge of 10^5 electrons/pixel. The 3-μm-wide, deeper CCD channel in the C register, in combination with a large electric-fringing field associated with the 10-μm-long CCD gates, appears to be responsible for the dramatic improvement of the charge-transfer efficiency over our previous design of the C register. The C register of the 160 x 244-element imager having 20-μm-long CCD gates, apparently without the benefit of fringing fields, exhibited relatively large transfer inefficiencies (in the range of 10^{-3} to 10^{-2}/transfer) at very low background charge levels. However, for operation with a 300-K background charge level, the new 160 x 244 imager showed negligible reduction of spatial resolution because of the charge transfer inefficiency.

The introduction of aluminum busses, for clocking of the vertical column register, provided a more uniform clock voltage across the B register of the imagers and allowed operation with low SBD bias voltages.

The major problem encountered in processing the first wafer lots of IR-CCDs with the new IR-CCD process, is the presence of dark-current spots that tended to increase in numbers with an increase of the SBD operating voltage above 2 to 3 V. The dark-current spots appear to be associated with abrupt doping

profiles of arsenic n^+ guard rings. Future processing of these devices with more graded or double-diffused n-type guard rings is expected to eliminate the observed dark-current spots.

A shot-noise-limited noise equivalent temperature (NEΔT) of 0.038°C was demonstrated for operation of the 320 x 244 imager, with a 300-K background, 30 frames/s, f/2.0 cold shield, and 3.4-μm long-pass filter.

Preliminary results on the 160 x 244 imagers confirm our previous data that readout noise in excess of the shot noise is associated with SBD dark current. However, a lower readout noise can be achieved with smaller size SBDs, by using our lower dark-current SBD process or operating at temperatures of less than 77 K.

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